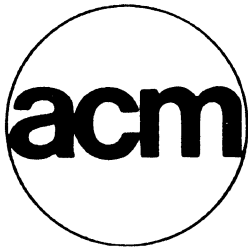


LIST 1974



SIGDA NEWSLETTER

SPECIAL INTEREST GROUP ON DESIGN AUTOMATION

Volume 4 Number 4 December 1974

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SIGDA dues are \$3.00 for ACM members and \$5.00 for non-ACM members. Checks should be made payable to the ACM and may be mailed to the SIGDA Secretary/Treasurer listed above, or to SIGDA, ACM Headquarters, 1133 Avenue of Americas, New York, N. Y. 10036. Please enclose your preferred mailing address and ACM Number (if ACM member).

SIG/SIC FUNCTIONS

Information processing comprises many fields, and continually evolves new subsectors. Within ACM these receive appropriate attention through Special Interest Groups (SIGs) and Special Interest Committees (SICs) that function as centralizing bodies for those of like technical interests ... arranging meetings, issuing bulletins, and acting as both repositories and clearing houses. The SIGs and SICs operate cohesively for the development and advancement of the group purposes, and optimal coordination with other activities. ACM members may, of course, join more than one special interest body. The existence of SIGs and SICs offers the individual member all the advantages of a homogeneous narrower-purpose group within a large cross-field society.

ACTIVITIES

- 1) Informal technical meetings at SJSS and FJCC.
- 2) Formal meeting during National ACM meeting + DA Workshop.
- 3) Joint sponsorship of annual Design Automation Workshop.
- 4) Quarterly newsletter.
- 5) Panel and/or technical sessions at other National meetings.

FIELD OF INTEREST OF SIGDA MEMBERS

Theoretic, analytic, and heuristic methods for:

- 1) performing design tasks,
- 2) assisting in design tasks,
- 3) optimizing designs through the use of computer techniques, algorithms and programs to:
 - 1) facilitate communications between designers and design tasks,
 - 2) provide design documentation,
 - 3) evaluate design through simulation,
 - 4) control manufacturing processes.

CHAIRMAN'S MESSAGE

Charles E. Radke

At the ACM Conference in San Diego on November 11, 1974, a handful of officers and interested SIGDA members discussed some problems facing SIGDA; but more important, we listed the opportunities within SIGDA and ACM. For once, the problems were few and the opportunities many.

NOMINATION AND ELECTION OF OFFICERS:

I have appointed a nominating committee headed by Dave Hightower along with Steve Krosner and Don Humcke. The term of the present officers expires the end of June. Your particular input and concerns can be sent to Dave Hightower. Your chance to vote comes in early 1975.

ACM 1974:

Those who attended had an opportunity to hear a variety of good papers and become stimulated under lively discussions. SIGDA had two well-received sessions in San Diego: (1) Data Base Systems for Design Automation Support, (2) Design Automation in the University.

ACM 1975:

Next year's ACM Conference is scheduled for October 20-22, 1975, in Minneapolis. What kind of sessions should SIGDA have? Do you have any suggestions? Any papers? (For submitting, use the form found elsewhere in the Newsletter.) Some suggestions proposed at the SIGDA meeting were:

1. Aids for Data Base Design
2. Design Methodology
3. System Specification Languages
4. Design Languages

At the SIGDA meeting it was pretty well agreed that SIGDA sessions at the ACM Conference should be directed toward the mainstream of ACM and workshops be used for more specific areas of DA. Your input is being solicited.

LECTURESHIPS:

Each year lecturers are appointed by ACM to talk to local ACM chapters around the world. ACM has asked the SIGs to submit names for consideration. Here is a prime opportunity.

DESIGN AUTOMATION WORKSHOP (12th ANNUAL):

The well known and popular DA workshop partially sponsored by SIGDA will be held in Boston on June 23-25, 1975. The call for papers is out; are your abstracts in?

WORKSHOP ON DATA BASES FOR INTERACTIVE DESIGN:

A workshop, directed at graphic and other terminal use in design and the management of design data, will be held in Waterloo, Ontario, Canada, September 15-17, 1975. Here SIGDA joins SIGGRAPH (SIG on Graphics), SIGMOD (SIG on Management of Data), and the University of Waterloo to attack

an area of growing concern as DA grows within industry.

WORKSHOP ON COMPUTER HARDWARE DESCRIPTION LANGUAGES:

This workshop is directed at those particularly concerned with system specification and general design languages used in the designing of digital processors. The workshop was first held in Rutgers University in 1973 then in Darmstadt, Germany in 1974. On September 6-7, 1975, the third workshop will be held in New York under joint sponsorship of City College of City University of New York, SIGARCH (SIG on Architecture), Computer Society (Technical Committee for Computer Architecture), and SIGDA.

SIGDA NEWSLETTER:

As you have noticed we have been meeting our committed publication schedule. At a meeting held in Denver at the DA workshop, many attendees requested regular publication so they could get letters and notes published. Here is your opportunity to let others know about your work and concerns. Do you have a brief article but you don't want to go through extended refereeing? If the item is reasonably short and in camera ready form, we'll consider printing it in the next issue of the Newsletter.

What is your involvement? The Special Interest Groups of ACM have been developed for the development and advancement of your special area of interest. SIGDA provides you with many opportunities.

You, I am sure, have something of interest to others in SIGDA. Maybe you don't think so, but we and others do. I suggest you jot down an outline of what you might say, approach your management for approval, discuss with your local peers, and work up a paper to present, a note for the SIGDA Newsletter, or a brief article for the Newsletter.

Take the opportunity; we would like to hear from you.

FROM THE EDITOR

This issue contains several announcements for meetings which have already been held. These were received too late for publication in the last issue and have been included for reference. I will gladly publish relevant meeting notices in the very next issue following receipt, but that's the best I can do!

The deluge of papers promised to the newsletter at the Denver DA Workshop has not materialized. Once more--we welcome working papers, project reports, meeting reviews and other material which might be of interest to SIGDA readers. An informal exchange of ideas is being encouraged by Dave Hightower in the Forum (page 29).

As can be deduced from contents of the last few issues, the influx of paper and book reviews has been less than overwhelming. If you've read a good (or bad!) paper lately, why not let the rest of the group know? If you have any suggestions for improving the newsletter, please let me know--this is a very informal publication!

Rob Smith

1974 DESIGN AUTOMATION WORKSHOP
CONFERENCE REPORT

BY D. J. HUMCKE

The 11th Annual Meeting of the Design Automation Workshop was held in Denver, Colorado, U.S.A., on June 17-19, 1974. Attending the conference were 300 representatives of university, government and industrial communities from Canada, France, Germany, Holland, Italy, Japan, Sweden and the U.S.A. Forty-six technical papers which encompassed the Design Automation discipline of six countries were presented during the three-day meeting.

Design Automation in the context of this meeting is the use of computers as tools which aid in the design process. It is often extended to include areas such as testing, simulation and certain segments of manufacturing. These areas are frequently referred to by synonymous terms such as Computer Aided Design (CAD), Computer Aided Manufacturing (CAM), machine aids, automated design, automated drafting, etc., and comprise portions of potentially totally integrated systems.

It is the purpose of this workshop or conference to provide a forum whereby developments in the field of Design Automation can be presented and discussed. It is the aim of this workshop to improve and expand the quality and quantity of Design Automation developments. Because of the breadth of subject matter, the three-day program has been arranged so that technical papers are presented concurrently in different disciplines of Design Automation. For some attendees with broad backgrounds there can be conflicts, but for most attendees there is something of interest throughout each day of the meeting.

Tutorial sessions are presented each day surveying the "state-of-the-art" of one of the areas in which technical papers will be presented during that day. The main purpose of the tutorials is to provide a broad background for the uninitiated in a particular area of Design Automation. This year, tutorials were conducted in partitioning, data base design, simulation and test generation, and interconnection. The tutorials are conducted by members of the discipline that have made recognized contributions to these fields.

Common interest groups convene after each day of formal presentations to informally discuss, in greater depth, the information and ideas presented throughout the day. Discussions involve such topics as circuit design, packaging, interconnection, testing, simulation, architecture, mechanical or whatever topic is of common interest to a group. It is at these meetings where innovation takes place.

The program this year was highlighted with a Keynote Speech by Dr. Steve Lukasik, Director of Advanced Research Projects Agency, U.S. Department of Defense. Dr. Lukasik's speech cited some of the current problems resulting from the use of computers, where we are going, what we may see in the future, some of the problems we may face and what can be done.

The current problems he cited were: (1) the privacy (and accuracy) of information in large data bases, (2) the reliability of hardware and software, (3) computer crime (of software and data), and (4) the inadequacy of current input/output techniques such as the use of alphanumeric terminals. Next he cited that what we are going to see in the near future are faster computers with larger memories, and a decline in the cost per executable instruction. Further in the future, we will find that computers as we know them today may disappear. They will either be absorbed into a product of some kind or will be available as very large systems which will be utilized like power stations. Dr. Lukasik stated that one of the problems we may face in the future is that computers will solve problems in such unorthodox ways that we will suspect the objective of the solution. For example, one might question if the optimization of the solution is oriented towards man or oriented towards the machine. Finally he cited some ways that we may prevent this from happening: (1) keep some information out of the computer, (2) maintain a working knowledge of the machine, and (3) restrict certain individuals from access to the machine.

The technical program consisted of 14 sessions with three or four papers presented in each session. Each presentation lasted approximately 20 to 25 minutes followed by a 5 to 10-minute discussion period. Some sessions were concluded with a panel discussion in which all attendees were invited to participate.

The first session consisted of presentations in the area of Large Scale Integration (LSI). A system approach to LSI design employed in Japan was described starting from logic description, and proceeding through placement, routing, artwork, and test generation utilizing an on-line graphical display. All functions operated from a common data file. Another presentation emphasized a production-proven IC design rule checking function which performed prescribed or user-specified physical description checks such as conductor width calculations and clearance checks.

Session 2 was one of two Graphics sessions consisting of presentations utilizing interactive graphic techniques. A presentation on the computer-aided process design and simulation for the forging of turbine blades pointed out the material savings that can be achieved through the proper design of molds using interactive graphic techniques. A description was given of an interactive

graphic system built from hierarchically-structured functions such that any subroutine along with the subroutines it calls can be removed without upsetting the functioning of any other chain in the program structure.

Session 3 covered topics in the area of circuit partitioning. An approach to the circuit partitioning problem utilizing interactive graphics to combine aspects of both an automated approach and a manual approach was described. It was stated that the results obtained are better than those obtainable by using either approach independently. A state-of-the-art survey of topological methods for solving the circuit layout problem was presented followed by a more detailed description of one model which allowed pin and gate assignment as a function of the layout. Finally, a technique was described which initially orders circuits according to a scoring mechanism and then uses a 2-stage interchange technique to arrive at a final partition.

Session 4 was the second session on Graphics. The first presentation described an artwork generation system for integrated circuits and printed wiring boards which utilized digitizers, interactive graphics, plotters, a design rule checker, and a pattern command program. This was followed by a description of an investigation that was made into automatic visual inspection systems for electronic assemblies. Three major phases were researched: scanning devices, software algorithms, and possible computer systems. Finally, a program and the associated command language for controlling automated mask analysis was described.

Session 5 covered the area of Documentation Systems. The documentation of schematics was described utilizing a system which provides the automatic placement and routing of circuit elements. Along with a 33 percent savings in cost, a shorter publication time and earlier start of the publication effort was cited. Other presentations on a printed wiring board and minicomputer design and documentation system described total design systems which yielded design documentation. The total design system approach appeared to be a main theme of the majority of the presentations that were made at this conference.

Session 6 covered the area of Test Data Generation. A description was given of how the data files of a series of programs which were developed over the years to completely automate the test cycle were combined. The output of these programs were a test deck for card driven test equipment accompanied by a listing of detected or undetected faults. In another instance, programs for test generation, fault simulation, and test minimization for combinational switching circuits which formed a special strategy directing the choice of a test set were described. The object is to minimize the number of tests required for the

detection of logical faults. Finally, a new algorithm for test generation for a sequential circuit with at least 1000 logic blocks was discussed. It is based on special values expressed in boolean vectors, their logical operators, and three basic theorems.

Session 7 on Function Design Techniques covered a variety of Design Automation techniques. A program which translated a purchase order for a computer into the required set of hardware and software components was described. A comparison of force directed placement techniques was presented. A method for modeling any two conductor transmission lines in terms of a SCEPTRE transient analysis program was described. A paper which critically analyzed the software development process was presented. Finally, some speculation on the future of Design Automation was presented. The speculation covered the areas of descriptive languages, partitioning, placement, routing, test generation, the data management system, and the effect of making logic or hardware changes.

Session 8 consisted of presentations in the area of Design Automation in the architectural field. Papers were presented on topics covering the planning for a new town, the generation of maps and a computer-aided land use study incorporating techniques by which site evaluations could be made with respect to land use. Finally, an experiment to replace the iterative computation approach with an interactive approach to an architectural design utilizing four basic interactive functions was described.

Session 9 covered topics in the area of Simulation. A report was presented of the problems encountered while functionally testing LSI gate arrays in a production environment. Some solutions which were being implemented to overcome these problems were offered. A presentation was made on techniques which were implemented for timing analysis and termination of fault-induced activity within an assignable delay digital fault simulation environment.

Session 10 covered some more General Applications of Design Automation. The Maritime Administration uses computer-aided techniques in ship design to meet its responsibility to assure that the preliminary design of ships meet design criteria such as speed and cargo capacity while insuring safety by answering such questions as "Will it float?" A description of a real-time minicomputer system for sign design, stencil making, payroll and timekeeping, file management, font design, maintenance, and hardware diagnostics was presented.

Session 11 included topics on the subject of interconnection. A paper was presented describing an iterative method of routing which tries to avoid crossings and path adjacency while simultaneously controlling path length. Described is an improvement algorithm which reroutes portions of the board in order to complete the routing. Another presentation discussed a method of assigning cost penalties to different aspects of interconnection, such as vias, length, horizontal and vertical segments, to determine the best route. Finally, an interactive design station for routing multilayer backplanes is described. The system uses a digitizer plotter, storage scope and standalone computer.

Session 12 consisted of topics in the area of Large Scale Design Automation Systems. Presentations in this session included a description of all the activities in arriving at a Design Automation System for aerospace vehicle design such as planning, design objectives and stages of design of the system's data base relationships. Another paper discussed the necessary attributes of Design Automation regarding the preliminary design of tactical weapons systems using interdisciplinary computer aids.

Session 13 covered topics in the area of Software. A presentation was made describing the tools (or programs) which make up a Design Automation System from conception to the finished product. Some examples of the tools are a descriptive input language, an interpreter, a data base, and interactive programming. Standard procedures, adding devices and management of the devices were discussed. In another presentation, the effects of job scheduling algorithms on computer system performance and resources are demonstrated and evaluated by a simulation model of a hypothetical, graphically distributed network computer.

Session 14, Design System Needs, consisted of presentations of advanced Design Automation Systems making extensive use of interactive capabilities and structured data base systems. The goal that was established was to evaluate present Design Automation tools, determine areas not yet attacked by Design Automation or areas where present Design Automation Solutions require improvement. The object is to develop techniques to deal with these problems. Some of the areas under investigation are: high-level hardware design languages, primitive hardware design languages, physical design languages, macros, partitioning, placement, and interconnection. Concluding this session was a presentation on a highly structured data base design and data management system to aid in the solution of the printed circuit board problem.

The 11th Design Automation Workshop had much to offer to the attendees throughout the day and night. One of the unique features of the workshop was the distribution of a 375-page bound copy of the proceedings during registration. The proceedings contain the complete paper for each of the presentations that are made at the conference. The proceedings can then be scanned to determine papers of interest and aid the attendees in formulating questions to pose to the speakers following their presentations.

Copies of the proceedings of the 11th Design Automation Workshop and other past workshop meetings can be obtained from either of the following organizations:

Association for Computing
Machinery
Order Department
P.O. Box 12105
Church Street Station
New York, New York 10249
U.S.A.

IEEE Computer Society
Attention: Mr. True Seaborn
5855 Naples Plaza
Suite 301
Long Beach, California 90803
U.S.A.

Either of these organizations should be contacted before placing your order to determine the cost and availability of past proceedings of individual meetings.

The 12th Design Automation Conference will be held at the Hilton Hotel in Boston, Massachusetts, on June 23-25, 1975. A "Call for Papers" is being made for presentations at this conference. Papers should be submitted to the Program Chairman no later than January 9, 1975. Papers should be no longer than 5000 words and should be accompanied by a 25-word abstract for the program brochure. Rough drafts will be accepted at this time. Papers to be reviewed for presentation at the 12th Design Automation Conference should be sent to Dr. Steven A. Szygenda, The University of Texas, Electrical Engineering Department (515), Austin, Texas 78712, U.S.A. Requests for detailed program information (when available) should be made to Mrs. Judith G. Brinsfield, Bell Laboratories, Room 3B-323, Whippany Road, Whippany, New Jersey 07981, U.S.A.

1974

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CONFERENCE ON COMPUTER AIDED GEOMETRIC DESIGN

Reported by Robert E. Barnhill
University of Utah

An international conference on Computer Aided Geometric Design was held at The University of Utah, Salt Lake City, 18-21 March 1974. It was attended by about 120 people, including several from Europe. University, industry, and government labs were all represented.

The topic of this conference involves both mathematics and computer science and is truly cross-cultural. Curve and surface design and description is the central theme of this subject.

In order to have sufficient flexibility, parametric representation of curves and surfaces is used. The paper by Peters is useful in obtaining an appropriate view of parametric definitions. Three important requirements for curve and surface representations are (1) smoothness, (2) local support, and (3) ease of computation. Cubic interpolatory B-splines provide excellent results for (1) and (2) and, with equally spaced knots, for (3). B-splines were discussed by Coons, Riesenfeld, and others. Forrest's talk was a survey of computational geometry. Bezier, Gordon, and Mehlum discussed their respective curve and surface representation systems. Both of these systems were developed to solve certain industrial problems and have also become topics of research interest elsewhere. Barnhill, Gregory, and McDermott reported on surface representations that are intrinsically bivariate, i.e., cannot be formed by tensor products of one variable schemes. Splines under tension were discussed by Nielson and Pilcher. Demonstrations were provided by Fred Parke: A discussion of the development of three-dimensional half-tone models for human faces that allow

- (1) reasonable approximation to real faces
- (2) facial expression.
- (3) speech synchronized facial animation

Ed Catmull: A demonstration of University of Utah shaded equipment by showing pictures of photographs mapped onto bicubic patches.

Jim Clark: A demonstration of a 3-D CAD system for B-spline surfaces. The system uses a 3-D head-mounted display and 3-D wand for interacting with the surfaces.

Ron Resch and Ephraim Cohen: The demonstration will include defining a curve by an arbitrary set of points and passing a spline through them. The defined curve is then declared to be a folded edge. The program then determines the required developable surfaces and displays the results. This demonstration will use an Imlac terminal connected to a PDP 10 computer.

Garland Stern: A demonstration of font creation and editing of special characters for terminal text.

Evans & Sutherland Demonstrations: The Picture System: Introduced commercially during the summer of 1973, The Picture System is the E & S standard product, stand-alone, real-time line drawing system.

Three-Dimensional Digitizing Tablet: Developed by Ivan E. Sutherland early in 1972, the Tablet employs two pens, has a large area and translates data from two-dimensional photographs via the pens to three-dimensional coordinates for the creation of shaded pictures.

Newspaper/Graphic Arts System: This system has been designed by Evans & Sutherland as an interactive display ad layout and news page makeup system with visual feedback to be interfaced with a basic composition system.

Computer Generated Visual Simulation System for Flight Training (NOVOVIEW): The NOVOVIEW System was developed by E & S for Redifon Flight Simulation Ltd., Crawley, England and provides real-time night scenes of lights representative of those seen at an airport and the surrounding areas.

The conference was supported by the Office of Naval Research, by the Mathematics Department, the Computer Science Department, and the Dean of Science at the University of Utah.

The proceedings of the conference will be published by Academic Press about the end of 1974 and they should be ordered directly from Academic Press.

The program of the conference follows:

S. A. Coons, Syracuse University, "Surface Patches and B-Spline Curves".

A. R. Forrest, University of Cambridge, England, "Computational Geometry - Achievements and Problems".

D. C. Evans, Evans & Sutherland Corp., "A Survey of Graphics at Utah".

R. E. Barnhill, University of Utah, "Smooth Interpolation over Triangles".

J. A. Gregory, University of Utah, "Smooth Interpolation without Twist Constraints".

R. J. McDermott, University of Utah, "Graphical Representation of Surfaces over Triangles and Rectangles".

R. F. Riesenfeld, University of Utah, "B-Spline Curves and Surfaces".

P. Bezier, Renault, Paris, "Mathematical and Practical Possibilities of UNISURF".

N. Max, "Computer Animation of Smooth Sur-

faces II".

G. M. Chaikin, NYU Aerospace Lab, "An Algorithm for High Speed Curve Generation".

J. W. Lewis, Yale, "Least Square Splines in Computer Aided Geometric Design".

R. F. Wieringa, Philips Research Lab., Eindhoven, Netherlands, "Constrained Interpolation Using Beier Curves as a New Tool in Computer Aided Geometric Design".

University of Utah Graphics Demonstrations.

Evans and Sutherland Demonstrations, 3 Research Road.

E. Mehlum, Central Institute for Industrial Research Oslo, "Nonlinear Splines".

G. M. Nielson, Arizona State University, "Polynomial Alternative to Splines in Tension".

D. T. Pilcher, Hercules, Inc., "Surfaces under Tension".

R. Resch, University of Utah and E. Cohen, Applicon, Boston, "The Space Curve as a Folded Edge".

G. J. Peters, McDonnell-Douglas, "Parametric Bicubic Surfaces".

M. Sterling, Systems Associates, Inc., "Computer Aided Design in the Auto Industry".

J. R. Manning, Shoe and Allied Trades Assoc., England, "Feature Lines on Curved Surfaces".

C. M. Strauss, Brown University, "Visualization of Complex-Valued Functions".

A. B. Navarro and D. A. Luther, Planning Research Corp., McLean, VA., "A Consolidated Interactive Graphics Systems".

W. J. Gordon, General Motors Research Lab., "Computer Aided Design and the Geometric Aspects of the Finite Element Method".

R. M. Flegal, Xerox, "Color Video Graphics as a Design Tool".

P. G. Kirmser and K. K. Hu, Kansas State University, "Two Dimensional Interpolation".

M. Newell, University of Utah, "Man-Machine Communication in Three Dimensions".

E. Catmull and R. Rom, University of Utah, "A Class of Local Interpolating Splines".



International Conference and Exhibition on Computers in Engineering and Building Design

Imperial College, London 25th–27th September 1974

PROGRAMME

This programme is based on the abstracts submitted to the conference organizers and may be modified when the full papers are received. Sessions are of two kinds: engineering application sessions and specialist sessions, marked thus: Displays*.

A final programme will be issued to all registered delegates shortly before the conference, together with full joining instructions. The registration desk at the conference will be open from 14.00 on 24th September.

REGISTRATION

Registration is £56 for the full conference (3 days) or £28 for a single day. The principal author of each paper, or the author who will deliver the paper at the conference, may register at the authors' rate of £48 for the full conference. Only one author may register at this rate for each paper. No special rate is given for single day registrations.

Full conference registration includes abstracts of the papers, an exhibition catalogue, lunches, dinners and refreshments, conference dinner and a copy of the proceedings.

One-day registration includes lunches, refreshments and abstracts of the papers. Please use the enclosed registration form. More copies are available from the Conference Organizers.

PAYMENT

Cheques should be made payable to IPC Business Press Ltd.

CANCELLATION

Registrations may be cancelled up to 31st August 1974 without charge. Delegates cancelling after this are likely to forfeit part or all of their conference fee.

PROCEEDINGS

The proceedings of the conference will be published in early 1975. Each three-day delegate will be sent one copy. Other copies will be on sale at a reduced price to authors. Details will be sent to all delegates in December 1974.

LANGUAGE

The conference language will be English.

MEALS AND REFRESHMENTS

Lunch, dinner and morning and afternoon refreshments will be provided in Imperial College, immediately beside the conference and exhibition halls.

TRAVEL

Wakefield Fortune Ltd, Thames House, Millbank, London SW1 have been appointed travel agents to the conference. Contact Mr B. Hearn. Telephone: 01 834 7253. Telex: 917596.

ENQUIRIES

Contact the Conference Organizers M.I. Dawes and G.W. Jones at: IPC House, 32 High Street, Guildford, Surrey, GU1 3EW England. Telephone: Guildford (0483) 71661. Telex: Scitechpress Gd 85556.

EXHIBITION

The exhibition will provide a concentration of c.a.d. equipment and know-how for the engineers who are considering how to use c.a.d. in their own projects.

An extensive array of the latest hardware, including plotters, display units, workstations, digitizers, minicomputers, disc and magnetic tape units and tape readers, will be shown, together with the latest in software packages for engineering and building design. The equipment on show will meet the needs of engineers in all branches of engineering, mechanical, civil, structural, chemical, electrical and electronic, as well as the specialist in c.a.d.

EXHIBITION CATALOGUE

Full details of the exhibition will be contained in a catalogue available shortly before the conference. All delegates will receive one free copy.

KEY DATES

19th August – final date for papers
31st August – last date for cancellation
24th–27th September – exhibition open
25th–27th September – conference held
Jan/Feb 1975 – conference proceedings published

Opening times:

Tuesday 24th:	14.00 – 18.00
Wednesday 25th:	10.00 – 18.00
Thursday 26th:	10.00 – 18.00
Friday 27th:	10.00 – 14.00

For more information contact the Exhibition Manager, T.G. McGowran at IPC House, 32 High Street, Guildford, Surrey GU1 3EW, England.

The conference is organized by *Computer Aided Design* in collaboration with:
Computer Aided Design Centre, Cambridge
Displays and C.A.D. Groups of the British Computer Society
Heat Transfer and Fluid Flow Service, Harwell

WEDNESDAY 25th SEPTEMBER

OPENING ADDRESS

Professor Sir Hugh Ford

D.O. ORGANIZATION AND DRAFTING

The computer's place in the drawing office
Speaker to be announced

PD3 - An automated drafting and circuit design package.
R.F. Allum (Bell Northern Research, Ottawa)

Computer-aided drafting *C.B. Besant and A. Jebb*
(Imperial College of Science and Technology, London)

A graphics database for engineering
B. Bittner and R. Wolf (Xerox Corporation, El Segundo/Rochester)

MORNING COFFEE

The role of automatic digitizers in c.a.d.
C.M. Williams (Virginia Polytechnic Institute)

Computer-aided construction of technical illustrations
C.J. Richards (Lanchester Polytechnic, Coventry)

Computer-aided drafting in the bridge design office
I. Hamilton (CAD Centre, Cambridge)

Multi-user digitizing systems in cartography
R.E. Grindley (Computer Equipment Co, UK)

MECHANICAL ENGINEERING

A system for the synthesis of machine structures
J.N. Siddall and D.J. Bonham (McMaster University, Ontario)

Computer-aided engine cam design
A. Sarsten (Université de Sherbrooke, Quebec)

Program package for large deflection analysis of twin rods and their assemblies
M. Konopasek (UMIST, Manchester)

SPREAD 3 - Finite element system for design and analysis of three-dimensional flat springs
J.R. Wolberg and Y. Glazer (Technion, Haifa)

ELECTRICAL AND ELECTRONIC ENGINEERING

An algorithm for the realization of a ternary logical function
R. Amer (Cairo University)

Circuit analysis programs in Europe and the USA
J.R. Greenbaum (General Electric Co, Syracuse)

Third generation computer-aided circuit analysis programs
J.R. Greenbaum (General Electric Co, Syracuse)

LUNCH INTERVAL

CIVIL ENGINEERING

SYTLIN - program for sight line calculation
D.G. Davies and R. Penn (BSC Port Talbot, Glamorgan)

Computer-aided design and analysis of prestressed concrete bridge decks
D. Bond (Queens University, Belfast)

RC - Building 1
A. Craddock (University of Technology, Loughborough)

Highway and structural c.a.d. using a Cadmac graphics terminal
P.B. Jeffreys (Mott, Hay and Anderson, Croydon)

GRAPHICS

Computer graphics in engineering design and manufacture
P. Aughton (BAC, Bristol)

Techniques for improving the role of graphics in c.a.d.
R.F. Allum (Bell Northern Research, Ottawa)

Computer graphics in the design and manufacture of node points in offshore oil rig substructures
S.A. Abbas (Teesside Polytechnic, Middlesbrough)

Interactive graphics - a little exploited medium for design
M.D. Apperley (Imperial College, London)

Interactive graphics in civil engineering - portability and adaptability
R.L. Schiffman et al (University of Colorado)

HEAT EXCHANGE AND FLUID FLOW

TASC1. A program for the design of shell-and-tube condensers
D. Butterworth and M.J.C. Moore (HTFS Harwell)

Computer-aided design of heat exchangers in a service organization to industry *M.J.C. Moore et al (HTFS, Harwell)*

The specification of circularly symmetric corrugated diaphragm configurations
D.L. Critten (Kent Instruments Ltd, Luton)

Shell-and-tube exchangers with condensation on the shell side
D. Chisholm and C. Cotchin (National Engineering Laboratory, East Kilbride)

AFTERNOON TEA

C.a.d. systems for the water engineer
V.P. Lane (General and Engineering Computer Services Ltd, Liverpool)

Optimal design with fixed geometry
H. Multamäki (Teknillinen Laskenta, Helsinki)

Computer simulation of lake networks
H. Sorvari (Teknillinen Laskenta, Helsinki)

The use of the computer in civil engineering design
M.R. Prince (Atkins Research and Development, Epsom)

Monitoring graphic techniques in design
D.S. Willey and D. Yeomans (University of Liverpool)

The travelling road sweeper *H.B. Humpidge (Sheffield, England)*

A computer program introducing size constancy in the plane representation of tri-dimensional objects
H.C. Ruggini (Buenos Aires)

Computer graphics in art and design
J.A. Vince (Middlesex Polytechnic, Enfield)

Interactive design of optical filters
A.C. Kilgour (University of Glasgow)

Computer animation *C. Yi et al (Imperial College, London)*

Calculation of shell side pressure drop for segmentally baffled shell and tube heat exchangers by divided flow method
I.D.R. Grant (National Engineering Laboratory, East Kilbride)

The thermal design of plate fin reboilers
T.D.A. Kennedy (HTFS, Harwell)

Mathematical modelling of radiant heat transfer
J.S. Truelove (HTFS, Harwell)

THURSDAY 26th SEPTEMBER			
09.00 – 10.30	CHEMICAL ENGINEERING	SEMICONDUCTOR DEVICES	GEOMETRICAL/SHAPE/SURFACE DESIGN ●
	Invited Review <i>J. Villadsen (Danish Technical University, Copenhagen)</i>	C.a.d. in semiconductor device problems <i>G. Pierini (CISE, Milan)</i>	Invited Review: surface and shape representation for c.a.d. <i>M.A. Sabin (BAC, Weybridge)</i>
	Computer-aided design of a reducing elbow for a penstock <i>V. Cugini et al (Institute of Mechanics and Machine Construction, Milan)</i>	The use of graph-theoretical methods for integrated circuit design <i>W.M. VanCleave (University of Waterloo, Ontario)</i>	Shape optimization of glass containers under external loads <i>M. Crochet (Unite de Mecanique Appliquee, Belgium)</i>
11.00 – 12.30	The dissemination of research expertise into chemical engineering industry <i>D.G. Howes and M.E. Leesley (SCICON/CAD Centre)</i>	Design of IMPATT diodes <i>S.R. Wilbur and D.L. Bates (University College, London)</i>	Some new shapes based on bicubic splines <i>J.G. Hayes (National Physical Laboratory, Teddington)</i>
		Large-signal transistor modelling <i>G.A. Richards (Marconi Research Laboratories, Great Baddow)</i>	Curve generation; a consideration of methods in relation to hardware implementation <i>D.W.H. Hampshire and R.C. Osbaldeston (Portsmouth Polytechnic,)</i>
MORNING COFFEE			
11.00 – 12.30	A user-oriented language and package for design of chemical processes <i>R.W.H. Sargeant (Imperial College of Science and Technology, London)</i>	BUILDING DESIGN AND ARCHITECTURE	Polynomial splines for both approximation and interpolation <i>E. Kantorowitz (Technion, Haifa)</i>
	A rational approach to distillation simulation <i>P. Winter (CAD Centre, Cambridge)</i>	HELP – housing evaluation layout package <i>C. Aybet (ABACUS, Strathclyde University, Glasgow)</i>	MANUFACTURING AND N.C. ●
	Thermal and stress analysis of an HTR vessel using graphics to display the model <i>B. Spooner (Atkins Research and Development, Epsom)</i>	An approach to computer-aided architectural design <i>B. David and V. Rivero (ENSIMAG, Grenoble)</i>	Invited survey <i>J. Hatvany (Computer and Automation Institute, Budapest)</i>
14.00 – 15.30		From British research in the building sciences towards French implementation <i>P.T. Daniel and F. Pavageau (Flintshire County Council/SERI)</i>	Computer aid in wing design <i>R.S. Davis (BAC, Weybridge)</i>
		Towards computer-aided design in a private architectural practice <i>J.A. Davidson (Gollins, Melvin, Ward & Ptnrs, London)</i>	Cutting of two-dimensional rectangular plates <i>N. Christofides (Imperial College, London)</i>
LUNCH INTERVAL			
14.00 – 15.30	CONTROL SYSTEMS	Program and data structures for computer-aided building <i>J.C. Gray (Applied Research of Cambridge)</i>	Invited review: c.a.d. in shipbuilding <i>R. Hurst (British Ship Research Association, Wallsend)</i>
	Invited review: Software for control system design <i>N. Munro (UMIST, Manchester)</i>	An integrated architectural c.a.d. system <i>A.D. Hamlyn et al (Imperial College, London)</i>	An artificial intelligence approach to manufacturing automation <i>R.T. Chien and T. Woo (University of Illinois)</i>
	C.a.d. of compensators for nonlinear control systems <i>R.H. Davis and E. Kraemer (Heriot-Watt University, Edinburgh)</i>	Building design <i>D. Kernohan (ABACUS Strathclyde University, Glasgow)</i>	C.a. manufacture of mechanical components using a simplified cutting sequence <i>M.H. Choudhury (Ferranti, Edinburgh)</i>
16.00 – 17.30	An interactive program package for data analysis, system identification and parameter estimation <i>M.J. Denham and L. Rigby (Imperial College, London)</i>	CASH – a computer-aided design tool for housing <i>K. Mathur (ABACUS, Strathclyde University, Glasgow)</i>	Computer-aided pipe production system <i>B. Dodd and J. Jack (Imperial College, London)</i>
	Classical control system design by interactive computer-aided methods <i>K.C. Daly et al (Imperial College, London)</i>	Interactive building design <i>A. Main</i>	
AFTERNOON TEA			
16.00 – 17.30	Interactive graphics in the design of nonlinear control systems <i>J.O. Gray (UMIST, Manchester)</i>	A rationalized approach towards architectural design <i>R. Th'ng (ABACUS, Strathclyde University, Glasgow)</i>	The application of c.a.d. techniques to machine tool design, production and manufacture <i>A. Jebb et al (Imperial College, London)</i>
	C.a.d. of industrial control systems <i>D.C. Williams (Warren Spring Laboratory, Herts)</i>	An experiment in computer-aided architectural design <i>J. Lansdown (Turner, Lansdown, Holt & Ptnrs London)</i>	The use of contours as an interface between c.a.d. and c.a.m. <i>D.G. Wilkinson (National Engineering Laboratory, East Kilbride)</i>
	The role of minicomputers in computer-aided system identification <i>P.E. Wellstead (UMIST, Manchester)</i>	A cost advice aid for the building design team <i>P. Purcell (Royal College of Art, London)</i>	Interactive c.a.d. in shipbuilding AUTOKON <i>F. Lillehagen (Central Institute for Industrial Research, Norway)</i>
	Modelling and control of an inverted pendulum using bond graphs <i>B.A. White et al (UMIST, Manchester)</i>	Automated architectural drafting system <i>K. Sakakibara (Nikken Sekkei Co, Tokyo)</i>	
	CADCUM – a computer-aided control system design suite <i>N. Munro (UMIST, Manchester)</i>	An historical cost benefit analysis of a computer system for architectural design <i>W.R. Laxon and J.J. Lefevre (Informatique et Batiment, Paris)</i>	
CONFERENCE DINNER			

FRIDAY 27th SEPTEMBER

STRUCTURAL ANALYSIS

Invited survey: structural analysis programs
G.M.J. Williams (Scott Wilson Kirkpatrick & Ptnrs, London)

Repeated stiffness analysis on a minicomputer
R.J. Cope (University of Liverpool)

Structural design on a minicomputer
R.J. Cope and J.H. Bungey (University of Liverpool)

Interactive graphics in structural analysis
W.S. Elliott and H.A. Lomke (Imperial College, London)

09.00 — 10.30

PROJECT MANAGEMENT

Information requirements of a design and consultancy organization
L.B. Cousins (HTFS, Harwell)

The PD3 system — project and document control
P.M. Gray (Bell Northern Research, Ottawa)

Problems of establishing a computer department within the professional design office
V.P. Lane (General and Engineering Computer Services, Liverpool)

Computer-aided concept, design and production — a look at systems solutions
R.K. Oatman (Computervision Cpn, Amsterdam)

The specification and development of c.a.d. systems: the relevance of task analysis
J. Wood (Royal College of Art, London)

TEACHING C.A.D.●

Minimum cost allocations of dimensional tolerances — an optimization problem for courses in mechanical engineering design
G. Ashton and J. Ellis (University of Salford)

The teaching of c.a.d.
D.W.H. Hampshire (Portsmouth Polytechnic)

The use of a matrix manipulative scheme in teaching of linear elastic analysis of structures
B.S. Lee (University of Newcastle)

C.a.d. in university courses
R.E. Radley (University of Sheffield)

Education in c.a.d. for post-graduates
D. Rzevski (Kingston-on-Thames Polytechnic)

MORNING COFFEE

INGA — an interactive graphic system for structural analysis
J. Greger (University of Stuttgart)

Interactive finite element data generation for three-dimensional plate structures
H.A. Nasreldin (University of Leicester)

The development of complex structures in the communications industry
A.T. Humphrey (Marconi Co, Chelmsford)

Computer aided analysis and design of steel frames
L.J. Faeber et al (Rensselaer Polytechnic Institute, New York)

11.00 — 12.30

BUILDING DESIGN: SERVICES AND STRUCTURES

Heating installation design in an integrated computer-aided building system
D.W. Archer (Applied Research of Cambridge)

The monitoring of service networks
R. Baxter and R. Brady (University of Cambridge/Applied Research of Cambridge)

Optimization of design parameters for refrigerated dehumidifiers using iterative simulation on a digital computer
A. Iqbal (Atkins Research and Development, Epsom)

Optimized silencing of high velocity air conditioning ducts
A. Iqbal and T.K. Wilson (Atkins Research and Development, Epsom)

OPTIMIZATION●

SEA — a new algorithm for the solution of nonlinear optimization problems
A.H. Goddard and A.D. Rowe (Imperial College, London)

NDC optima
S.E. Hersom (Hatfield Polytechnic, Herts)

Optimization as a design tool
R.M. Filmer (Building Research Establishment, Watford)

Application of optimization techniques in communications systems
M.H.E. Ward (Pye Telecommunications Ltd, Cambridge)

Sub-optimal solutions to combinatorial design problems
A.D. Pearman (University of Leeds)

LUNCH INTERVAL

DISPLAYS●

Invited survey: Interaction with visual information
D.J. Grover (NRDC, London)

The HRD-1: a high resolution storage display
G.S.B. Street (Laser Scan Ltd, Cambridge)

A microprogrammed processing module for displays
D.J. Woollons (University of Sussex, Brighton)

14.00 — 15.30

The design of portal frames by computer to strength and deflection requirements
D. Anderson (University of Warwick)

Structure evaluation in a closed building method
H.M. Evans (Applied Research of Cambridge)

Building design
D.M. Curtis (Oscar Faber and Ptnrs, St. Albans)

Computer optimization for studying summertime temperatures in buildings
R. Jones (Building Research Station, Watford)

RELIABILITY●

Reliability assessment in computer-aided design
R.N. Allan (UMIST, Manchester)

Using c.a.d. for reliability improvement
A.A. Kaposi and C.D. Partridge (Kingston Polytechnic, Surrey)

A program to calculate mean time between failures
A.H. Boyce (Marconi Research Laboratories, Great Baddow)

AFTERNOON TEA

Displays and medical physics
J. Clifton (University College Hospital, London)

Methods of using resources
H. Smith (University of Sheffield)

16.00 — 17.30

BIBRACS — an integrated computer system for architectural use
D.H. Mountford (Brockhouse Steel Structures Ltd, West Bromwich)

Grafting interactive graphics onto an existing batch system for architectural design
W.R. Laxon (Informatique et Batiment, Paris)

Design of building structures using a minicomputer c.a.d. system
P.M. McIntock et al (Imperial College, London)

Progress in the development and evaluation of CEDAR, a computer-aided building design system
B.G.J. Thompson (Property Services Agency, Croydon)

MANAGEMENT/GENERAL

Methods for improving consumer acceptance of c.a.d. programs
G.M. Mills (University of Bradford)

Security of data in c.a.d. systems — a cipher technique
D.L. Williams (Bell Northern Research, Ottawa)

Modelling the design process
G.L. Mallen (Royal College of Art, London)

Decentralized development for design automation
T.M. Korelitz (The Badger Company, Cambridge Mass.)

CUBE (Computer Use By Engineers) **SYMPOSIUM** **CALL FOR PAPERS**

PURPOSE

The goal of this symposium is to accelerate the exchange of information about the use of computers in advancing engineering technology. This exchange should benefit AEC research and development laboratories and help engineers bring to bear the latest techniques in computer use by:

- Sharing engineering computer codes among the laboratories.
- Creating an awareness of the current development of engineering codes.
- Discussing common problems and approaches in using computers.
- Exploring methods for more effective and efficient utilization.
- Stimulating creativity in computer use.

SUMMARY OF CUBE SYMPOSIUM PROGRAM

Wednesday, October 23

- 9:00 - 9:10 AM - Welcome by Dr. Roger Batzel
- 9:10 - 10:40 AM, Session 1 - COMPUTER FACILITIES REVIEW - Auditorium
- 11:00 - 12:00 Noon, Session 2 - COMPUTER GRAPHICS - Auditorium
- 1:00 - 2:15 PM, Session 3A - MECHANICAL ENGINEERING ANALYSIS I - Auditorium
- 1:00 - 2:20 PM, Session 4 - PROCESS CONTROL - Bldg. 111 Briefing Room
- 2:45 - 4:45 PM, Session 3B - MECHANICAL ENGINEERING ANALYSIS II - Auditorium
- 2:50 - 4:50 PM, Session 5 - DATA ACQUISITION - Bldg. 111 Briefing Room

Thursday, October 24

- 9:00 - 10:15 AM, Session 6 - CODE DEVELOPMENT I - Auditorium
- 9:00 - 10:15 AM, Session 9 - DATA ANALYSIS - Bldg. 111 Briefing Room
- 10:45 - 12:00 Noon, Session 7A - NETWORK ANALYSIS I - Auditorium
- 10:45 - 12:00 Noon, Session 10 - SYSTEMS ANALYSIS - Bldg. 111 Briefing Room
- 1:00 - 2:20 PM, Session 7B - NETWORK ANALYSIS II - Auditorium
- 1:00 - 2:15 PM, Session 11 - MECHANICAL ENGINEERING COMPUTER AIDED DESIGN - Bldg. 111 Briefing Rm.
- 2:50 - 4:40 PM, Session 8 - DIGITAL DESIGN - Auditorium
- 2:45 - 4:15 PM, Session 12 - CODE DEVELOPMENT II - Bldg. 111 Briefing Room

Friday, October 25

- 9:00 - 10:20 AM, Session 13A - MANAGEMENT & PHILOSOPHY I - Auditorium
- 9:00 - 10:30 AM, Session 14 - SIGNAL PROCESSING & NETWORK ANALYSIS III - Bldg. 111 Briefing Rm.
- 10:50 - 12:00 Noon, Session 13B - MANAGEMENT & PHILOSOPHY II - Auditorium

CENTRE D'ETUDES ET DE RECHERCHES
DE L'ECOLE NATIONALE SUPERIEURE DE L'ARCHITECTURE
ET DE L'ESPACE



UN COMPUTER AIDED DESIGN SYSTEMS

10 - 11 DECEMBER 1974

Approved by _____

- DELEGATION A L'INFORMATION
- and DIRECTION DES RECHERCHES ET MOYENS D'ESSAIS

TUESDAY, DECEMBER 10, 1969

9 AM Welcome - Registration
10 AM Attention by H. VERBORGEN - Director of the HUMAN and CERN
Introduction by H. HANSEN - 'Indagation & Informations'

KARLSRUHE, R.F.A.

19.10/31.30 AN
GERMINAL : towards a general and integrated
system for C A B
R. JACQUART, P. ROZIER, P. R. VALETTE, ORNHA-
CENT, Toulouse, France
Presentation of main goals of the system.
Description of the system : language, database,
interaction with applications programs, interactive
programming.

Questions

11.45/10.45 AM
MINIAN : a general programming system for
scientific and technical use
Olef KAYSER, Denmark : Ingenterstadet, Lyngby,
Denmark.

Main features of the system are discussed : the different language levels, integration of application programs, data grouping - implementation of the system.

Questions

... (PANELS)

2/3/40 PW	QUESTIONS FOR C A D EIGHTH
	A. J. LAURENCE, C A D Centre, Cambridge, N.E.
3/40/3.40 PW	QUESTIONS
3/40/3.10 PW	BASIC SOFTWARE TOOLS FOR C A D
3/40/3.10 PW	ETPO (Graphics Software)
	G. C. FRANKLIN, C A D Centre, Cambridge, N.E.
3/31/3.10 PW	QUESTIONS
3/30/4.10 PW	MAINBODY : early version of an integrated C A D system
	J. SIEGEL, C A D Centre, Cambridge, N.E.
4/10/4.10 PW	QUESTIONS
4/30/4.10 PW	MEMOIR

Content of the Narrative

U. JALLAINT

Administrative Services Unit

THURSDAY, DECEMBER 11, 1974

SESSION III - PRESENTATION : M.A. SABIN (B.A.C.)
MEYERHOLZ, U.K.

FUNCTIONS AND STRUCTURE OF THE INFORMATION

SYSTEM FOR TECHNOLOGY : I S F

Professor Jan PAUL, Technische Universität

Description of the functions of the system management, subsystem management, file management, data management, procedure management and command management of the IS7. Presentation of the essential features of the internal logic of the IS7 nucleus. Methodology of subsystem development with examples from practice

QUESTIONS

ABSTRACT : a P L I based integrated C A D system
Docteur SCHLECHENDANK - Kernforschungszentrum/
IfR, Karlsruhe, R.F.A.

The following points will be emphasized:

- system philosophy and concepts, module management, data base system, dynamic arrays,
- the PL2-procedural language, problem-oriented language definition and processing.

Questions

SESSION IV : PANEL DISCUSSION

PRESIDENT : M. BAILEY (THOMSON CAP, PRESIDENT OF THE FRENCH CHAPTER OF THE ACR)

Introduction by the President

The panelists who are potential users will
critique and comment the works presented at
along the three preceding sessions.

Notes

**Fénel allocation from M. BANSAY,
Director des Recherches et Moyens d'Enquête**

12th Annual

DESIGN AUTOMATION WORKSHOP



***** BOSTON, MASSACHUSETTS *****

REQUIREMENTS FOR SUBMITTING PAPERS

If you plan to submit a paper, you should send three copies of the paper (rough drafts are acceptable) to the program chairman no later than January 2, 1975.

Accompanying the draft should be the full name, address, and telephone number of the principal author, with whom all further direct communication will be conducted.

Notification of acceptance will be sent to you during the first week of February, 1975. After notification of acceptance, you will receive detailed instructions on the format to be observed in typing the final copy. To insure the availability of Proceedings at the Workshop, your final manuscript will be due April 21, 1975.

Final papers should be no longer than 5000 words, and the presentation should be limited to 20 minutes. Projection equipment for 35mm slides and viewgraph (overhead projector) foils will be available for every talk. Please indicate what, if any, additional audio-visual aids you require.

Program Chairman

Rough drafts are to be sent to the Program Chairman:

S. A. Szygenda
The University of Texas
Electrical Engineering Department (ENS 515)
Austin, Texas 78712
512-471-7365

Chairman of 12th DAW
R. B. Hitchcock

Sponsors

The sponsors of the Design Automation Workshop are the ACM (Association for Computing Machinery) Special Interest Group on Design Automation and IEEE (Institute of Electrical and Electronics Engineers) Computer Society.

Design Automation

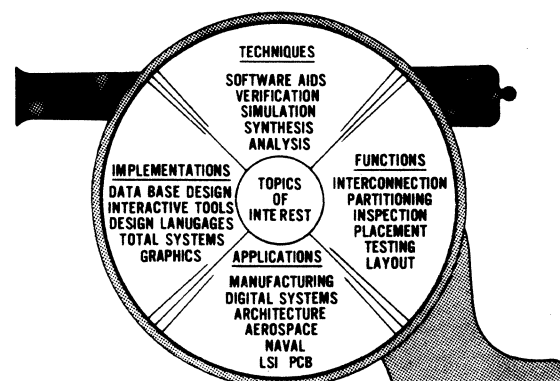
Design Automation implies the use of computers as aids to the design process.

In the broadest sense, the design process includes everything from specifying the characteristics of a product to meet a marketing objective to enumerating the details of how it is to be manufactured and tested.

Thus design automation embraces applications from one end of the design process to the other.

Site of 12th DAW

Statler Hilton Hotel
Park Square at Arlington Street
June 23, 24, 25, 1975



CALL FOR PAPERS

Workshop on Computer Hardware Description Languages and Their Applications

September 3-5, 1975
New York City, New York USA

Increasing interest and attention have been given to the areas of computer-aided logic/system design and documentation. A good computer hardware description language (CHDL) can be used for describing, documenting, simulating and implementing digital systems. The 1973 and 1974 workshops have been held in New Jersey, and West Germany respectively. The Third Workshop on CHDL will be held the week before the 1975 COMPON (September 9-11, Washington, D.C.)

Papers in the following and related areas will be considered:

1. New concepts for description languages
2. Constructs and mechanisms in computer descriptive languages
3. Comparison of languages
4. Applications of languages in documentation, simulation and hardware implementation
5. Hardware compiler (translator) implementation
6. System simulation
7. Computer-aided logic synthesis, logic synthesizer implementation
8. Experience on using languages, simulators, translators and logic synthesizers
9. Analysis of Digital Systems
10. Different levels of CHDL
11. Future prognosis

Information regarding the Workshop can be obtained from:

Professor Stephen Y. H. Su
Workshop Chairman
Department of Electrical Engineering
The City College, City University of New York
New York, N.Y. 10031
Telephone: (212) 621-2392
(212) 621-2248 (secretary)

You are invited to submit 3 copies of the paper in 10 to 20 double-spaced typewritten pages to: Professor Donald L. Dietmeyer

Department of Electrical and Computer Engineering
University of Wisconsin
Madison, Wisconsin 53706
Telephone: (608) 262-3890, 262-3840

The deadling for submitting the papers is March 1, 1975. The papers will be reviewed by the referees.

There will be a session for presenting the most recent results. Authors who would like to talk in this session should submit two copies of the summary to Dr. Dietmeyer by June 1, 1975. Papers for this session will not be published in the Proceedings.



**Sponsored by
ACM/SIGDA
SIGMOD/SIGGRAPH**

September 15-17, 1975

**University of Waterloo
Ontario, Canada**

PUBLICATION

Papers accepted for presentation at the workshop will be published in a volume of workshop proceedings. This will be presented to participants at the workshop registration.

If you are interested in participating in this workshop, you are invited to submit a paper for presentation. Please send notice of your intention to submit a paper and a brief statement of the paper's main points by January 20, 1975 to:

Dr. Robin Williams
Program Chairman
IBM Research Division (K54/282)
Monterey & Cottle Roads
San Jose, California 95193, USA

CALL FOR PAPERS

Workshop on Data Bases For Interactive Design

Many computer-aided design systems operate on large volumes of graphical and non-graphical data. Special consideration must be given to data base management systems and working data subsets. A need exists for standardization data base organizations in business and scientific applications.

In this spirit SIGDA, SIGGRAPH, and SIGMOD (the special interest groups of the ASSOCIATION FOR COMPUTING MACHINERY for Design Automation, Graphics, and Management of Data) in co-operation with the University of Waterloo are jointly sponsoring a workshop which will bring together designers who use large quantities of data and computer scientists who develop the interactive data base and graphics systems. The workshop is intended to explore mutual areas of interest and to promote an understanding of inter-related problems.

TOPICS

- Data Base Management Systems and their potential application in computer assisted design.
- Interactive computer graphics systems including data base support.
- Design automation involving large volumes of data.
- Data distribution in design applications (intelligent satellites, data networks).

OBJECTIVES

- Stimulate the development of data base technology and its potential applications in design.
- Examine the role of interactive graphics in the design data base environment.
- Provide a forum for interaction between computer scientists and those involved in the design process.

IMPORTANT DATES

- January 20, 1975 — Notice of intention to submit a paper due.
- March 15, 1975 — First draft of manuscript; 5000 words or less, due for review.
- May 15, 1975 — Authors notified of acceptance of papers.
- July 1, 1975 — Final revision of manuscript due.
- September 15-17, 1975 — Workshop meets at the University of Waterloo, Ontario, Canada.



NATIONAL CONFERENCE
OCTOBER 20-22, 1975
RADISSON HOTEL • MINNEAPOLIS, MINNESOTA

PRELIMINARY CALL FOR PAPERS

Deadline for submission of technical papers to ACM '75 is 1 March 1975. The technical program will consist of sessions organized by ACM Special Interest Groups and Committees, as well as sessions devoted to special topics of current interest (such as Microprocessors, Computing Networks, Finance/Banking), tutorials, and student papers.

You are invited to indicate your interest in submitting a paper for ACM '75 by sending the completed coupon below to:

J. B. Rosen
Technical Program Chairman, ACM '75
114 Main Engineering Building
University of Minnesota
Minneapolis, Minnesota 55455

Additional detailed information will be sent you when we receive your expression of interest.

I plan to submit a paper to ACM '75 in the following general category:

- ☐ 1. Computer Hardware and Architecture
- ☐ 2. Software
- ☐ 3. Mathematical Aspects of Information Processing
- ☐ 4. Systems for Management and Administration
- ☐ 5. Applications to Science, Technology and Humanities
- ☐ 6. Student Paper Competition
- ☐ 7. Other Topic of Current Interest

DESIGN AUTOMATION

Indicate SIG/SIC Category (if appropriate) SIGDA

The tentative title of my paper is _____

Name _____

ACM or other affiliation _____

Address _____

City _____ State _____ Zip _____

S I G M O D

(Formerly SIGFIDET)

INTERNATIONAL WORKSHOP MANAGEMENT OF DATA: DESCRIPTION, ACCESS AND CONTROL

MAY 14-16
San Francisco Bay Area

The fourth annual Workshop on the Management of Data sponsored by SIGMOD (formerly SIGFIDET) will be held in the San Francisco Bay Area on May 14-16 1975, prior to the National Computer Conference.

The objectives of the workshop are to 1) classify the basic issues in the utilization, development and processing of data bases and 2) present relevant research on and solutions to recognized data base problems. Discussion by active practitioners on the presented papers will take place in the form of audience interaction, forums and working sessions.

Suggested topics for this workshop include, but are not necessarily limited to, the following:

- Data Base Access, Design, Requirements, Recovery and Privacy
- Data Base Reorganization: Restructuring and Reformatting
- Data Translation (Methodology, Research and Practice)
- Data Definition Languages
- Data Dictionaries
- Data Structures
- Data Base Management Systems: Relational, Network, Hierarchical
(Utilization, Design, Evaluation Requirements)
- User Views of Data (End user → System Programmer)

YOUR HELP IS REQUESTED

Members of the University of Oklahoma Student ACM Chapter are making up a list of particularly good computing articles undergraduate and beginning graduate students should read.

THE MAIN CRITERIA SEEM TO BE:

1. The author should know what he is talking about and should express it well.
2. The paper should be understandable to a college senior majoring in mathematics and/or computing sciences.

Please suggest articles which you feel students would benefit from reading.

A copy of their final list will be sent to those recommending articles. It should be informative to see what students recommend that students read -- and what they omit.

Send your suggestions to:

Richard V. Andree
601 Elm, Room 423
The University of Oklahoma
Norman, Oklahoma 73069

The FORUM

Starting with this issue we are carrying a regular feature called The FORUM. Its purpose will be to provide a formal medium through which readers may exchange ideas, critique articles appearing in the newsletter (or elsewhere for that matter), and answer other FORUM letters. Address your letters to The FORUM and mail them to me. I will start the ball rolling with the following view point.

For as long as I can remember, developers of design automation systems (for electronic circuits) have had as their goal the elimination of manual layout of circuits. What do we have to show for that effort? Systems that are really very inadequate when applied to real, everyday circuits.

The best inroads into real automation of design have come in the areas of thin film or MOS/LSI - but what about the printed wiring board? Who can say they have a DA system that can handle a general class of PWB's - DIP's, discretes, transformers, capacitors, various ways of distributing power and ground, etc.?

Now, who can say they worked on such a system - everybody! Maybe much of that work was wasted. Maybe we would have been much further ahead if we had been working instead on better tools for the draftsman. Imagine if all development work on PWB DA systems had been geared toward better tools rather than toward doing the complete job automatically. We would be getting out PWB's much faster.

We are beginning to see such systems now (Foster, Calafiore, "A System for MultiLayer Printed Wiring Layout", 1974 DA Workshop), and I suggest we should have been designing these systems all along.

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A RESPONSE

Here at LLL we're exploring the approach of using an interactive graphics terminal to develop a (potentially incomplete) design specification in terms of logic schematics and mechanical layout diagrams. The graphics design file would then be processed by programs which would add details and produce various types of outputs.

The schematic data entry scheme appears attractive for several reasons. First, the set of schematic and mechanical layout blueprints are the basis for all design, fabrication and maintenance work here. Manual translation of rough design schematics into any other format represents needless extra work. This approach also permits orderly evolution of a system which would eventually provide a wide spectrum of services, requiring less and less information to be manually provided during design data entry.

It appears that many designers prefer to develop rough designs in schematic form. Therefore, interaction using any non-graphical medium would require a tedious translation or abstraction process, clearly an undesirable situation.

It is not presently clear that the capital expenditure necessary to provide this service is justifiable, but we are certain that such a capability could be developed. More information concerning this system will be available shortly.

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Review of Structural Mechanics
Computer Programs

In June, University Press of Virginia published Structural Mechanics Computer Programs, Surveys, Assessments, and Availability. The book contains most of the papers presented at the International Symposium on Structural Mechanics Computer Software which was held at the University of Maryland from 12 - 14 June.

Some structural engineers, architects, and mathematicians have referred to this book as a bible. Time will tell if they are correct. Certainly many of the papers do contain descriptions of systems and programs. For instance, there is a paper on GEVESYS, which is a machine-independent software sharing system. Also, there are several papers like "Nonlinear Continua" by Van Risemann, Stricklin, and Haisler. This paper presents an abstract of over forty computer programs and contains an appendix which lists the source of 33 programs.

A few other papers proceed in the same vein. Yet not all structural programs are similarly treated, or even mentioned. Nor is all the information completely correct. Still, this book deserves commendation, if only for its unique attempt to provide a single source of information.

Many of the programs in this book are universal enough to appeal to all programmers. Plus there are survey papers which should be beneficial to both the scientific and business computer communities, such as the one by Jackie Potts - a founder of SIGGRAPH - entitled "For the Computer Gourmet - Graphics." It covers the history and present state-of-the-art of the entire computer graphics field. To those who use it wisely, this book should provide a savings of both time and money.

There are two indexes. The first is a subject index of structural mechanics computer programs without any page numbers. If a desirable program is found, its page number must be located in the second index. This is an alphabetical listing giving page numbers. Unfortunately, there is not title or author index. Hopefully this omission will be corrected in future printings.

There are 1105 pages. The book sells for \$20 from the University Press of Virginia, Charlottesville, Virginia.

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Jackie Potts
Executive Committee SIGGRAPH
Code 1745
Structures Department
Naval Ship Research & Development Center
Bethesda, Md.

Paper Review--

Routeing according to a Structured Biplanar Scheme
in Printed Boards," G. Alia, G. Frosini and P. Maestrini,
Computer Aided Design, Vol. 5 No. 3 (July 1973), pp. 152-159.

The problem described involves placement and interconnection of a single module type on two layer boards. Modules are assigned to one side of the board, with the legal locations forming a uniform grid. A channel-type routine scheme is used, with horizontal and vertical channels on separate layers.

The procedures described seek to minimize conducting path area, hence (indirectly) total path length. Via count and engineering constraints are apparently not considered.

Module placement starts with decomposition of the modules into column sets, using connectivity within and between column sets as the basis for partitioning. Connectivity within column set is used to determine relative positioning within column. Column adjacency determination resembles some force-directed placement schemes, although column orientation appears to have been arbitrary.

A conventional channel router scheme is used to determine interconnection paths. The technique was implemented in APL on a S/360-67. The following results are extracted from the text of the paper. A pseudo-random problem containing 6 rows and 7 columns of legal locations contained 42 modules (14 pins each).

		<u>MIN</u>	<u>SEC</u>
Placement	Column Assignment	3	36
	Module Exchanges	30	1
	Module Ordering	3	51
	Column Ordering	1	11
Interconnection	Horizontal Segment Distribution	0	34
	Horizontal Segment Assignment	0	39
	Vertical Segment Assignment	<u>2</u>	<u>47</u>
	Total	42	39

The system required 20,000 bytes of memory, according to the authors.

Based on experimental analysis, the authors conclude that the module exchange phase of column (cluster) assignment is unjustified and should be omitted.

Rob Smith

To be published in COMPUTER, December 1974

A Survey of Computer Hardware Description Languages in U.S.A.⁺

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New York, N. Y. 10031

ABSTRACT

One important goal in digital engineering is to find a language which is descriptive, efficient for simulation and automatic hardware implementation purposes.

In this paper, the different levels of CHDL (computer hardware description languages) are introduced. Existing CHDL are surveyed and the features of these languages are pointed out. A table lists the names of CHDL, the authors, and the references. It also points out what language each CHDL is adapted from and reports the status of the implementation of these languages. Suggestions for overcoming the difficulties of using CHDL for computer-aided system/logic design are given.

+ This work is supported by the City University of New York Faculty Research Program under Grant No. 10597.

A Bibliography of Theses on Digital Design Automation.

by W.M. vanCleave
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University of Waterloo
Waterloo, Ontario, Canada

This bibliography contains most of the doctoral dissertations in the area of design automation of digital systems. A number of master's theses is also included. For most doctoral theses, a reference is made to the issue of Dissertation Abstracts, containing a description of the thesis and the University Microfilms order number is included. When known, the NTIS (National Technical Information Service) accession number is given.

An index by area as well as an index by degree-granting institution follow the listing.

- 1 ABEL, L.C.
ON THE AUTOMATED LAYOUT OF MULTI-LAYER PLANAR WIRING
AND A RELATED GRAPH COLORING PROBLEM.
UNIV OF ILLINOIS, DEPT OF COMPUTER SCIENCE,
PHD THESIS, COORD. SCIENCE LAB (CSL) REPT R-546, JAN 1972
- 2 APTE, R.M.
DERIVATION OF NEAR MINIMAL TEST SETS AND FAULT PARTITIONING
TECHNIQUES
SOUTHERN METHODIST UNIV, PHD THESIS, 1973; SUP: S.A. SZYGENDA;
DISS ABSTR, VOL 34, NO 8, P 3782B; UNIV MICROFILMS 74-5164.
- 3 ASHKINAZY, A.H.
FAULT DETECTION IN ASYNCHRONOUS SEQUENTIAL MACHINES
PHD THESIS, COLUMBIA UNIV, NY, 1970
- 4 BARAY, M.B.
A LANGUAGE FOR AUTOMATED LOGIC DESIGN
PHD THESIS, UNIV OF CALIFORNIA, BERKELEY, 1970, 125 PP ;
DISS ABSTR, VOL 31, NO 10, P 5920B ; UNIV MICROFILMS, NO 71-9760
- 5 BEARNSON, L.W.
DESIGN OF MINIMUM FAULT TEST SCHEDULES AND TESTABLE REALISATIONS
FOR COMBINATIONAL LOGIC CIRCUITS
PHD THESIS, AUBURN UNIV, 1970, 149 P; DISS ABSTR, VOL 31, NO 6,
P 3386B; UNIV MICROFILMS NO 70-22627; SUP: C.C. CARROLL.
- 6 BEDNAR, G.M.
AN ASYNCHRONOUS CIRCUIT DESIGN LANGUAGE SYSTEM
UNIV OF MISSOURI, ROLLA, PHD THESIS, 1972, 157 P;
DISS ABSTR, VOL 34, NO 8, P 3782B; UNIV MICROFILMS 74-4337.
- 7 BELT, J.E.
A HEURISTIC SEARCH APPROACH TO TEST SEQUENCE GENERATION FOR AHPL
DESCRIBED SYNCHRONOUS SEQUENTIAL CIRCUITS
UNIV OF ARIZONA, PHD THESIS, 1973, 208 P; SUP: F.J. HILL;
DISS ABSTR, VOL 34, NO 3, P 1102B; UNIV MICROFILMS NO 73-20626
- 8 BENGTSON, A.H.
ACHIEVING FAULT TOLERANCE THROUGH INHERENT REDUNDANCY TECHNIQUES
IN SMALL MICROPROGRAMMED COMPUTERS
PHD THESIS, PURDUE UNIV, 1972, 229 P; DISS ABSTR, VOL 33, NO 9,
P 4273B; UNIV MICROFILMS NO 73-5987; SUP: F.W. MOWLE
- 9 BORGSTAHL, R.W.
DIGITAL SYSTEM DESIGN AND SIMULATION
PHD THESIS, IOWA STATE UNIV, 1972, 116PP, SUP A.V. POHM;
DISS ABSTR, VOL 33, NO 8, P 3643B; UNIV MICROFILMS NO 73-3859.

- 10 BOSSEN, D.C.
SELF-DIAGNOSABLE DECOMPOSITION OF SEQUENTIAL MACHINES
PHD THESIS, NORTHWESTERN UNIV, 1968, 67 PP; DISS ABSTR,
VOL 29, NO 7, P 2428B; UNIV MICROFILMS NO 69-1789
- 11 BOSWELL, F.R.
A DIAGNOSTIC COMPUTER SYSTEM FOR FAULT DIAGNOSIS OF DIGITAL
CIRCUITS
PHD THESIS, CASE WESTERN RESERVE UNIV, 1972, 244 PP.
DISS ABSTR, VOL 33, NO 4, P 1496B ; UNIV MICROFILMS NO 72-26138
- 12 BOUTE, R.T.
FAULTS IN SEQUENTIAL MACHINES : ALGEBRAIC PROPERTIES AND
DETECTION METHODS
PHD THESIS, STANFORD UNIV, DEPT OF EL.ENG., 1973, 335P
DISS ABSTR, VOL 33, NO 12, P 5818B; UNIV MICROFILMS NO 73-14866.
- 13 BRADSHAW, F.T.
STRUCTURE AND REPRESENTATION OF DIGITAL COMPUTER SYSTEMS
PHD THESIS, CASE WESTERN RESERVE UNIV, 1971, 246 P ;
DISS ABSTR, VOL 32, NO 5, P 2648B ; UNIV MICROFILMS NO 71-22783.
ALSO: REPT 1114, JENNINGS COMPUTER CENTER, CASE WESTERN RESERVE
UNIV, JAN 1971
- 14 BREUFER, M.A.
THE USE OF MATHEMATICAL PROGRAMMING IN THE IMPLEMENTATION OF
BOOLEAN SWITCHING FUNCTIONS
PHD THESIS, UNIV OF CALIFORNIA, BERKELEY, 1964
- 15 BROWN, K.F.
THE USE OF INTERACTIVE COMPUTER GRAPHICS FOR TEACHING ELEMENTARY
NETWORK ANALYSIS
UNIV OF UTAH, PHD THESIS, 1973, 281 P; SUP: R.E. STEPHENSON;
DISS ABSTR, VOL 34, NO 7; UNIV MICROFILMS 74-177.
- 16 BROWN, T.J.
AN AUTOMATED DIGITAL DESIGN LANGUAGE FOR CLODS (COMPUTERIZED
LOGIC-ORIENTED DESIGN SYSTEM)
AIR FORCE INST OF TECHNOLOGY, WRIGHT PATTERSON AFB, OHIO, SCHOOL
OF ENGINEERING, MASTER'S THESIS, JUNE 1973, 198 P;
ALSO REPORT NO GE/EE/73S-1; NTIS AD 768 346/ 8GA
- 17 BURNETT, G.J.
DESIGN LANGUAGE FOR DIGITAL SYSTEMS
MIT, DEPT OF EL ENG, M.S. THESIS, AUG 1965
- 18 CANNON, D.L.
COMPUTER-AIDED INTEGRATED CIRCUIT RELIABILITY ANALYSIS
PHD THESIS, UNIV OF HOUSTON, 1970, 268 PP ; DISS ABSTR, VOL 31,
NO 12, P 7286B ; UNIV MICROFILMS NO 71-15466
- 19 CANTER, L.H.
TEST SEQUENCE GENERATION FOR MICROELECTRONIC CIRCUITS
UNIV OF SOUTHERN CALIFORNIA, PHD THESIS, 1973, 280 P;
SUP: I. REED; DISS ABSTR, VOL 34; UNIV MICROFILMS 73-31331
- 20 CARROLL, J.J.
EXAMINATION OF SEQUENTIAL CIRCUITS - A MODEL AND A METHOD
PHD THESIS, ILLINOIS INSTITUTE OF TECHNOLOGY, 1972, 107 P;
DISS ABSTR, VOL 33, NO 8, P 3644B; UNIV MICROFILMS NO 73-3620;
SUP: H.P. MESSINGER AND G.A. FISHER.
- 21 CARTER, E.A.
FAULT TEST GENERATION FOR SEQUENTIAL CIRCUITS DESCRIBED
IN AHPL
UNIV OF ARIZONA, PHD THESIS, 1973, 183 P; SUP: F.J. HILL;
DISS ABSTR, VOL 34, NO 11; UNIV MICROFILMS 74-11209
DIGITAL DESIGN LANGUAGE/AHPL
- 22 CAVALLO, M.B.
DIGITAL COMPUTER SIMULATION FOR DESIGN APPLICATIONS
NAVAL ACADEMY, ANNAPOLIS, MD, TRIDENT SCHOLAR REPORT, MAY 1973;
ALSO REPT USNA-TSPR-39; NTIS AD 769 504/ 2GA

- 23 CHANG, L.C.
COMPUTER SYSTEMS DIAGNOSIS USING GRAPH THEORY
UNIV OF TEXAS, AUSTIN, MASTER'S THESIS, MAY 1970
- 24 CHANG, L.C.
SOME DIAGNOSTIC APPROACHES FOR COMPUTER SYSTEM DESIGN
PHD THESIS, UNIV OF TEXAS, AUSTIN, 1972, 102PP
SUPERVISOR C.V. RAMAMOORTHY
DISS ABSTR, VOL 33, NO 9, P 4274B; UNIV MICROFILMS NO 73-7528.
- 25 CHAPPELL, S.G.
AUTOMATIC TEST GENERATION FOR ASYNCHRONOUS DIGITAL CIRCUITS
NORTHWESTERN UNIV, PHD THESIS, 1973, 139 P;
DISS ABSTR VOL 34, NO 9; UNIV MICROFILMS 74-7722
- 26 CHEN, F.T.
AN ALGORITHM FOR THE MINIMISATION OF TWO-LEVEL MULTIPLE-OUTPUT NETWORKS
PHD THESIS, UNIV OF ILLINOIS, URBANA-CHAMPAIGN, 1970, 139 PP
DISS ABSTR VOL 31, NO 5, P 2620B ; UNIV MICROFILMS NO 70-20938
- 27 CHESAREK, D.J.
FAULT DETECTING EXPERIMENTS FOR SEQUENTIAL MACHINES
PHD THESIS, STANFORD UNIV, 1972, 187 PP, DEPT OF EL ENG;
DISS ABSTR VOL 33, NO 5, P 2071B ; UNIV MICROFILMS NO 72-30607
- 28 CLEGG, F.W.
ALGEBRAIC PROPERTIES OF FAULTS IN LOGIC NETWORKS
PHD THESIS, STANFORD UNIV, DEPT OF EL ENG, 1970, 184 PP ;
DISS ABSTR VOL 31, NO 8, P 4678B ; UNIV MICROFILMS NO 71-2745
- 29 COHEN, D.J.
COMPUTER BASED FAULT ANALYSIS OF DIGITAL SYSTEMS
REPT CSRR-2020, UNIV OF WATERLOO, DEPT OF APPLIED ANALYSIS
AND COMPUTER SCIENCE, 1970 (PH D THESIS)
- 30 CORK, R.C.
AUTOMATIC TEST VECTOR GENERATION
MASTER'S REPT, DEPT OF INDUSTRIAL ENG, ARIZONA STATE UNIV,
FEB 1972
- 31 CRALL, R.F.
IDDAF - INTERACTIVE COMPUTER ASSISTANCE FOR CREATIVE DIGITAL DESIGN
PHD THESIS, UNIV OF MISSOURI, ROLLA, 1970, 70 PP ; DISS ABSTR
VOL 32, NO 3, P 1561B ; UNIV MICROFILMS NO 71-22386
- 32 CUSTEAU, G.R.
ASPECTS OF THE DESIGN OF MAINTAINABLE COMPUTERS
UNIV OF WATERLOO, PHD THESIS, 1971
- 33 CUTLER, A.B.
COMPUTER DESIGN OF INTEGRATED NPN TRANSISTORS
MASTER'S THESIS, ARIZONA STATE UNIV, SEP 1969
- 34 DANIELSON, G.H.
APPLICATIONS OF LINEAR GRAPH THEORY TO AUTOMATED NETWORKS LAYOUT
PHD THESIS, SYRACUSE UNIV, 1969, 125 PP; DISS ABSTR VOL 30,
NO 12, P 5494B ; UNIV MICROFILMS NO 70-10334
REPT R69ELS73, GENERAL ELECTRIC CO, ELECTRONICS LAB, SYRACUSE
- 35 DARRINGER, J.A.
THE DESIGN, SIMULATION AND AUTOMATIC IMPLEMENTATION OF DIGITAL COMPUTER PROCESSORS
PHD THESIS, DEPT OF COMPUTER SCIENCE, CARNEGIE MELLON UNIV,
MAY 1969, 333 P
DISS ABSTR, VOL 30, NO 5, P 2169B; UNIV MICROFILMS, NO 69-19088
- 36 DAS, P.
FAULT DETECTION EXPERIMENTS ON STRUCTURALLY DECOMPOSABLE SEQUENTIAL MACHINES
PHD THESIS, CLARKSON COLLEGE OF TECHNOLOGY, 1973, 97 PP;
SUP : D.E. FARMER ; DISS ABSTR, VOL 34, NO 1, P 173B;
UNIV MICROFILMS, NO 73-14850

- 37 DAS, S.
 FAULT-TOLERANT DIGITAL SYSTEMS USING FAIL-SAFE LOGIC
 WASHINGTON UNIV, D.S.C. THESIS, 1973, 190 P; SUP: Y.H. CHUANG
 AND R.O. GREGORY; DISS ABSTR, VOL 34, NO 12;
 UNIV MICROFILMS 74-13803
- 38 DAVIDSON, E.S.
 AN ALGORITHM FOR NAND DECOMPOSITION OF COMBINATORIAL SWITCHING
 FUNCTIONS
 PHD THESIS, UNIV OF ILLINOIS, 1968, 242 PP ; DISS ABSTR VOL 29,
 NO 7, P 2431B ; UNIV MICROFILMS NO 69-1329
 ALSO: REPT R-382, COORD SCIENCE LAB, UNIV OF ILLINOIS, JUNE 1968
- 39 DAVIS, R.F.
 FAULT TESTING IN COMBINATORIAL AND SEQUENTIAL TREE CIRCUITS
 PHD THESIS, WASHINGTON STATE UNIV, 1972, 219 PP, SUP K.C. WANG
 DISS ABSTR VOL 32, NO 12, P 6979B ; UNIV MICROFILMS NO 72-18511
- 40 DEPOLIGNAC
 UTILISATION DU LANGUAGE CASSANDRE POUR LA CONCEPTION DES
 MACHINES MICROPROGRAMMEES
 THESIS, UNIV DE GRENOBLE, 1973
- 41 DEVANEY, M.J.
 FAULT DIAGNOSIS AND SELF-REPAIR IN OPERATIONAL SYNCHRONOUS DIGITAL
 SYSTEMS
 PHD THESIS, UNIV OF MISSOURI, COLUMBIA, 1971, 249 PP;
 SUP G.V. LAGO ; DISS ABSTR VOL 32, NO 5, P 2702B; UNIV MICROFILMS
 NO 71-30641
- 42 DIEPHUIS, R.J.
 FAULT ANALYSIS FOR COMBINATIONAL LOGIC NETWORKS
 PHD THESIS, MIT, DEPT OF EL ENG, SEPT 1969
- 43 DIRECTOR, S.W.
 AUTOMATED NETWORK DESIGN ; PRINCIPLES AND TECHNIQUES
 PHD THESIS, UNIV OF CALIFORNIA, BERKELEY, 1968, 276 PP ;
 DISS ABSTR VOL 29, NO 12, P 4652B ; UNIV MICROFILMS NO 69-10279
- 44 DIXON, A.H.
 ON THE EFFECT OF CLIQUE DETECTION IN GRAPHS
 UNIV OF BRITISH COLUMBIA, PHD THESIS, 1973;
 DISS ABSTR, VOL 34, NO 12
- 45 DU, M.W.
 MULTIPLE FAULT DETECTION IN COMBINATIONAL CIRCUITS
 PHD THESIS, DEPT OF COMPUTER SCIENCE, JOHN HOPKINS UNIV, 1972
- 46 DULEY, J.R.
 DDL - A DIGITAL SYSTEM DESIGN TRANSLATOR
 PHD THESIS, UNIV OF WISCONSIN, 1967, 221 P, SUP D.L. DIETMEYER
 DISS ABSTR VOL 28, NO 8, P 3282B ; UNIV MICROFILMS NO 67-12116
- 47 EDGECOMBE, J.A.
 MICROPROGRAM SIMULATION.
 UNIV OF WATERLOO, MASTER'S THESIS, 1971
- 48 FARMER, D.E.
 FAULT DETECTION EXPERIMENTS FOR SEQUENTIAL MACHINES
 PHD THESIS, POLYTECHNIC INST OF BROOKLYN, 1970, 100 PP ,
 SUP E.J. SMITH ; DISS ABSTR VOL 31, NO 6, P 3325B ;
 UNIV MICROFILMS NO 70-26042
- 49 FIGUEROA, M.A.
 ANALYSIS OF LANGUAGES FOR THE DESIGN OF DIGITAL COMPUTERS
 MASTER'S THESIS, UNIV OF ILLINOIS ; ALSO REPT R-611, MAY 1973,
 133 PP ; NTIS AD762381
- 50 FIKE, J.L.
 HEURISTIC AND ADAPTIVE TECHNIQUES FOR DIAGNOSTIC TEST GENERATION
 PHD THESIS, SOUTHERN METHODIST UNIV, 1972, 215 PP, SUP
 S.A. SZYGENDA ; DISS ABSTR VOL 33, NO 12, P 5764B ;
 UNIV MICROFILMS NO 73-14472

- 51 FLETCHER, A.J.
COMPUTER PROGRAMS FOR THE LAYOUT OF INTEGRATED CIRCUITS
PHD THESIS, UNIV OF MANCHESTER, 1970
- 52 FLOMENHOFT, M.J.
ALGEBRAIC TECHNIQUES FOR FINDING TESTS FOR LOGICAL FAULTS IN
DIGITAL CIRCUITS
LEHIGH UNIV, PHD THESIS, 1973, 105 P;
DISS ABSTR, VOL 34, NO 11; UNIV MICROFILMS 74-11346
- 53 FOIK, F.F.
INTERACTIVE GRAPHICS INTERFACE FOR DIGITAL LOGIC SIMULATOR
MASTER'S THESIS, AIR FORCE INST OF TECHNOLOGY, WRIGHT PATTERSON
AFB, OHIO, SCHOOL OF ENGIN, MARCH 1973, 171 PP (NTIS AD760530)
- 54 FOLEY, J.D.
OPTIMUM DESIGN OF COMPUTER DRIVEN DISPLAY SYSTEMS.
UNIV OF MICHIGAN, SYSTEMS ENGINEERING LAB, REPT 34,
ANN ARBOR, 1968 (PHD THESIS), 274 P
DISS ABSTR, VOL 30, NO 5, P 2171B; UNIV MICROFILMS, NO 69-18002
- 55 FRANKE, E.A.
AUTOMATED FUNCTIONAL DESIGN OF DIGITAL SYSTEMS
PHD THESIS, CASE WESTERN RESERVE UNIV, 1967, 166 P ;
SUP: H. MERGLER; DISS ABSTR, VOL 29, NO 1, P 181B;
UNIV MICROFILMS, NO 68-10156
- 56 GABOW, H.N.
IMPLEMENTATION OF ALGORITHMS FOR MAXIMUM MATCHING OF
NONBIPARTITE GRAPHS
STANFORD UNIV, PHD THESIS, 1974, 248 P;
DISS ABSTR, VOL 34, NO 12; UNIV MICROFILMS 74-13628
- 57 GAULT, J.W.
THE APPLICATION OF FAULT INDISTINGUISHABILITY IN COMBINATIONAL
NETWORKS
PHD THESIS, UNIV OF IOWA, 1969, 101 PP, SUP J.P. ROBINSON
DISS ABSTR VOL 30, NO 9, P 4131B ; UNIV MICROFILMS NO 70-4362
ALSO: REPT THEMIS-UI-TR-13, JULY 1969 (NTIS AD 692 420)
- 58 GENTRY, M.L.
A COMPILER FOR COMPUTER HARDWARE EXPRESSED IN MODIFIED APL
PHD THESIS, UNIV OF ARIZONA, 1971, 137 PP, SUP F.J. HILL
DISS ABSTR VOL 32, NO 3, P 1499B ; UNIV MICROFILMS NO 71-24908
- 59 GORMAN, D.F.
A SYSTEM DESCRIPTIVE LANGUAGE
PHD THESIS, UNIV OF PENNSYLVANIA, DEPT OF EL ENG, APRIL 1968, 346P
DISS ABSTR, VOL 29, NO 7, P 2435B; UNIV MICROFILMS, NO 69-110
- 60 GOSTELOW, K.P.
LOGIK - A SYSTEM FOR THE COMPUTER-AIDED SELECTION AND ASSIGNMENT
OF ELECTRONIC MODULES
UCLA, DEPT OF ENG, REPT 68-8, MARCH 1968
- 61 GRAY, F.G.
FAULT TOLERANCE, DETECTION AND LOCATION IN ABSTRACT COMBINATIONAL
NETWORKS
PHD THESIS, UNIV OF MICHIGAN, 1971, 340 PP, SUP J.F. MEYER
DISS ABSTR VOL 32, NO 7, P 3943B ; UNIV MICROFILMS NO 72-4882
- 62 GRISWOLD, V.M.
VECTOR GENERATION FOR FAULT DIAGNOSIS IN LOGIC CIRCUITS
ARIZONA STATE UNIV, PHD THESIS, 1974, 140 P;
DISS ABSTR, VOL 34, NO 11; UNIV MICROFILMS 74-10713
- 63 GROENIG, S.R.
SELF FAULT DETECTION IN ASYNCHRONOUS SEQUENTIAL CIRCUITS
MS THESIS, UNIV OF IDAHO, 1971

- 64 HANEY, F.M.
USING A COMPUTER TO DESIGN COMPUTER INSTRUCTION SETS
PHD THESIS, CARNEGIE MELLON UNIV
- 65 HARTMAN, D.W.
AN ALGORITHM FOR FAULT DETECTION IN SYNCHRONOUS SEQUENTIAL
CIRCUITS
MASTER'S THESIS, MIT, DEPT OF EL ENG, JUNE 1968
- 66 HAYES, J.P.
A STUDY OF DIGITAL NETWORK STRUCTURE AND ITS RELATION TO FAULT
DIAGNOSIS
PHD THESIS, UNIV OF ILLINOIS, URBANA CHAMPAIGN, 1970, 141 PP
DISS ABSTR, VOL 31, NO 9, P 5366B ; UNIV MICROFILMS NO 71-5122
ALSO: UNIV OF ILLINOIS, CSL, REPT R-467, MAY 1970 (NTIS AD 707691)
- 67 HEMMING, C.W.
FUNCTIONAL SIMULATION TECHNIQUES FOR DESIGN VERIFICATION AND
FAULT INSERTION IN ELECTRONIC DIGITAL SYSTEMS
PHD THESIS, SOUTHERN METHODIST UNIV, CS/OR CENTER, SEPT 1971, 126 P
DISS ABSTR, VOL 32, NO 3, P 4590B ; UNIV MICROFILMS, 72-6358
- 68 HEMPHILL, J.M.
THE DEVELOPMENT OF PROCEDURES FOR THE ANALYSIS AND SYNTHESIS OF
A HIGHLY DEFINED CLASS OF FAULT TOLERANT COMPUTER SYSTEMS
PHD THESIS, SOUTHERN METHODIST UNIV, 1971, 127 PP, SUP
S.A. SZYGENDA ; DISS ABSTR VOL 32, NO 8, P 4532B ; UNIV MICROFILMS
72-6359
- 69 HOOVER, L.R.
SECONDARY TECHNIQUES FOR INCREASING FAULT COVERAGE OF FAULT
DETECTION TEST SEQUENCES FOR ASYNCHRONOUS SEQUENTIAL NETWORKS
PHD THESIS, UNIV OF MISSOURI, ROLLA, 1972, 76 PP ; DISS ABSTR
VOL 34, NO 1, P 220B ; UNIV MICROFILMS NO 73-17064
- 70 HORNFECK, W.A.
EFFICIENT GENERATION OF MINIMUM FAULT TEST SCHEDULES FOR
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PHD THESIS, AUBURN UNIV, 1971, 189 PP, SUP C.C. CARROLL;
DISS ABSTR VOL 32, NO 6, P 3356B; UNIV MICROFILMS NO 72-679
- 71 HOULE, J.L.
A FORMAL LANGUAGE FOR DESCRIBING DIGITAL SYSTEMS
UNIV OF WATERLOO, PHD THESIS, 1974
- 72 HSIEH, E.P.
OPTIMAL CHECKING EXPERIMENTS FOR SEQUENTIAL MACHINES
ENG SC D THESIS, COLUMBIA UNIV, NY, 1968
- 73 JAGADEFSAN, M.N.
MINIMISATION OF EXCLUSIVE -OR AND LOGICAL- EQUIVALENCE CIRCUITS
SC.D. THESIS, WASHINGTON UNIV, 125 PP, 1971, SUP Y.H. CHUANG &
D.F. WANN ; DISS ABSTR VOL 32, NO 2, P 939B ; UNIV MICROFILMS
NO 71-19844
- 74 JAUCH, H.E.
A NEW ALGORITHM FOR DETECTING FAULTS
UNIV OF MINNESOTA, PHD THESIS, 1973, 120 P;
DISS ABSTR, VOL 34, NO 11; UNIV MICROFILMS 74-10526
- 75 JOHNSON, D.B.
ALGORITHMS FOR SHORTEST PATHS
CORNELL UNIV, PHD THESIS, 1973, 162 P;
DISS ABSTR, VOL 34, NO 7; UNIV MICROFILMS 73-31823
- 76 KAMAL, S.
DIAGNOSIS OF INTERMITTENT FAULTS IN DIGITAL SYSTEMS
PHD THESIS, MICHIGAN STATE UNIV, 1972, 156 PP ; DISS ABSTR
VOL 33, NO 11, P 5241B ; UNIV MICROFILMS NO 73-12748
- 77 KAWASAKI, T.
OPTIMAL NETWORKS WITH NOR-OR GATES AND WIRED-OR LOGIC
UNIV OF ILLINOIS, DEPT OF COMPUTER SCIENCE, MASTER'S
THESIS, JAN 1974, 104 P; ALSO REPT DCS-R-74-623;
NTIS PB 228 474/ 3GA

- 78 KERNIGHAN, B.W.
SOME GRAPH PARTITIONING PROBLEMS RELATED TO PROGRAM SEGMENTATION
PHD THESIS, PRINCETON UNIV, 1969, 171 PP ; DISS ABSTR, VOL 30,
NO 5, P 2177B ; UNIV MICROFILMS NO 69-18168
- 79 KIME, C.R.
A FAILURE DETECTION METHOD FOR SEQUENTIAL CIRCUITS
DEPT OF EL ENG, UNIV OF IOWA, REPT 66-13, JAN 1966
(PHD THESIS)
- 80 KLAYTON, A.R.
FAULT ANALYSIS FOR COMPUTER MEMORY SYSTEMS AND COMBINATIONAL
LOGIC NETWORKS
PHD THESIS, LEHIGH UNIV 1971, 181 PP; DISS ABSTR VOL 32,
NO 5, P 2710B ; UNIV MICROFILMS NO 71-27723
- 81 KNUDSEN, M.J.
PMSL - AN INTERACTIVE LANGUAGE FOR SYSTEM LEVEL DESCRIPTION AND
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PHD THESIS, CARNEGIE MELLON UNIV, 1972, 262 P
DISS ABSTR, VOL 34, NO 3, P 1067B; UNIV MICROFILMS NO 73-21081
ALSO NTIS AD762 513
- 82 KO, D.C.C.
SELF CHECKING OF MULTIPLE OUTPUT COMBINATIONAL CIRCUITS
USING FORCED PARITY TECHNIQUE
UNIV OF SOUTHERN CALIFORNIA, PHD THESIS, 1973, 157 P;
SUP: M.A. BREUER; DISS ABSTR VOL 34, NO 7;
UNIV MICROFILMS 73-31361
- 83 KOHAVI, I.
FAULT DETECTION EXPERIMENTS FOR LOGICAL NETWORKS
PHD THESIS, POLYTECHNIC INST OF BROOKLYN, 1970, 108 PP
SUP E.J. SMITH ; DISS ABSTR, VOL 31, NO 7, P 4047B ; UNIV
MICROFILMS NO 70-26071
- 84 KOVIJANIC, P.
AN INTERACTIVE SYSTEM AS A TOOL FOR AUTOMATED LOGICAL DESIGN
CASE WESTERN RESERVE UNIV, MASTER'S THESIS, 1973
- 85 KREINICK, S.J.
A COMPUTER PROGRAM TO DESIGN PRODUCTION SPECIFICATIONS FOR
INTEGRATED CIRCUIT TRANSISTORS
MASTER'S THESIS, IOWA STATE UNIV, FEB 1970
- 86 LAMBERT, A.G.
IICADS - INTEGRATED INTERACTIVE COMPUTER AIDED DESIGN SYSTEM
PHD THESIS, UNIF OF MISSOURI, ROLLA, 1972, 86 PP ; DISS ABSTR,
VOL 34, NO 1, P 222B ; UNIV MICROFILMS, NO 73-17087
- 87 LANDGRAFF, R.W.
FAULT DETECTION, LOCATION AND RECOVERY ALGORITHMS IN THE DESIGN
OF MAINTAINABLE SYSTEMS
PHD THESIS, NORTHWESTERN UNIV, 1970, 127 PP ; DISS ABSTR, VOL 31,
NO 10, P 5980B ; UNIV MICROFILMS, NO 71-10146
- 88 LEAVENE, R.W.
ASYNCHRONOUS COMPUTER SIMULATION OF DIGITAL NETWORKS
UNIV OF MISSOURI, COLUMBIA, PHD THESIS, 1972, 162 P; SUP G.V.LAGO
AND R.A.WAID; DISS ABSTR, VOL 34, NO 3, P 1106B; UNIV MICROFILMS,
NO 73-21450
- 89 LEE, S.M.
STRUCTURE AND DIAGNOSIS OF SEQUENTIAL MACHINES
UNIV OF MISSOURI, COLUMBIA, PHD THESIS, 1972, 74 P;
DISS ABSTR, VOL 34, NO 3, P 1106B; UNIV MICROFILMS, NO 73-21452

- 90 LEKKOS, A.A.
FUNCTIONAL SIMULATION TECHNIQUES FOR A TIME DOMAIN INTERCHANGEABLE
FUNCTIONAL AND GATE-LEVEL SIMULATION ENVIRONMENT
PHD THESIS, SOUTHERN METHODIST UNIV, 1972, 181P (SUPERVISOR
S.A. SZYGENDA) ; DISSERTATION ABSTRACTS, VOL 33, NO 9, P 4234B,
MARCH 1973, UNIVERSITY MICROFILMS, ORDER NO 73-5202
- 91 LEWIS, R.S.
AN APPROACH TO TEST PATTERN GENERATION FOR SYNCHRONOUS SEQUENTIAL
CIRCUITS
PHD THESIS, SOUTHERN METHODIST UNIV, 1967, 129 PP, SUP F.W. TATUM
DISS ABSTR, VOL 29, NO 3, P 1007B ; UNIV MICROFILMS, NO 68-11843
- 92 LIBERMAN, A.B.
A SYSTEM FOR COMPUTER AIDED SYNTHESIS OF DIGITAL LOGIC CIRCUITS
D.FNG. THESIS, UNIV OF DETROIT, 1968, 139 PP ; DISS ABSTR, VOL 30,
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- 93 LIDDELL, P.
DECOUPAGE SYNTAXIQUE DE SYSTEMES LOGIQUES DECRITES EN CASSANDRE
THESIS, UNIV OF GRENOBLE, MARCH 1970
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SYNTHESIS OF LOGIC NETWORKS WITH MOS COMPLEX CELLS
PHD THESIS, UNIV OF ILLINOIS, 1972, 232 PP ; DISS ABSTR, VOL 33,
NO 10, P 4761B ; UNIV MICROFILMS, NO 73-9885
- 95 LUKES, J.A.
COMBINATORIAL SOLUTIONS TO PARTITIONING PROBLEMS
PHD THESIS, STANFORD UNIV, 1972, 130 PP ; DISS ABSTR, VOL 33,
NO 5, P 2081B ; UNIV MICROFILMS, NO 72-30665
- 96 MANDELL, R.L.
TOOLS FOR THE CONSTRUCTION OF DESIGN AUTOMATION SYSTEMS
PHD THESIS, UCLA, 1968 & UCLA REPT 68-6, JAN 1969
UNIV MICROFILMS, NO 69-5335
- 97 MARIN, M.A.
INVESTIGATIONS OF THE FIELD OF PROBLEMS FOR THE BOOLEAN ANALYSER
PHD THESIS, UCLA, 1968, 187 P, SUP: A.SVOBODA;
DISS ABSTR, VOL 29, NO 6, P 2040B; UNIV MICROFILMS, 68-16560
- 98 MARTINEK, A.
COMPUTER-GENERATED PRINTED CIRCUIT ARTWORK
M.A.SC. THESIS, UNIV OF WATERLOO, DEPT OF MECHANICAL ENG.,
APRIL 1970
- 99 MEHTA, M.A.
A METHOD FOR OPTIMIZING THE DIAGNOSTIC RESOLUTION OF INPUT/OUTPUT
FAULTS IN DIGITAL CIRCUITS
PHD THESIS, ILLINOIS INST OF TECHNOLOGY, 1971, 227 PP; SUP: H.P.
MESSINGER & W.B. SMITH ; DISS ABSTR, VOL 32, NO 11, P 6402B ;
UNIV MICROFILMS, NO 72-16188
- 100 MERNET, J.
DEFINITION DU LANGAGE CASSANDRE
THESIS, IMAG, UNIVERSITE DE GRENOBLE, MARCH 1970
- 101 MERNET, J.
ETUDE METHODOLOGIQUE DE LA CONCEPTION ASSISTEE PAR ORDINATEUR
DES SYSTEMES LOGIQUES : CASSANDRE
D.SC. THESIS, UNIV DE GRENOBLE, APRIL 1973
- 102 MICKELSON, C.T.
A REVISED HARDWARE LOGIC SIMULATOR
M.S. THESIS, CASE WESTERN RESERVE UNIV, 1969
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COMBINATORIAL ORDERING AND THE GEOMETRIC EMBEDDING OF GRAPHS
MIT - LINCOLN LAB, TECHNICAL NOTE 1971-35, AUG 1971 ; ALSO:
PHD THESIS, HARVARD UNIV (REPT ESD-TR-71-243)

- 105 NOBLIN, J.B.
A COMPARISON OF THE VARIOUS METHODS OF FAULT DETECTION
PHD THESIS, MISSISSIPPI STATE UNIV, 1972, 121 PP, DEPT OF EL ENG,
SUP R.D. GUYTON; DISS ABSTR, VOL 33, NO 12, P 5831B;
UNIV MICROFILMS, NO 73-13619
- 106 OESTREICHER, D.
AUTOMATIC PRINTED CIRCUIT BOARD DESIGN
PHD THESIS, UNIV OF UTAH, DEPT OF CS, REPT UTEC-CSC-72-119,
JUNE 1972; ALSO: NTIS AD 762 021
- 107 OMOHUNDRO, W.E.
FLOWWARE - A FLOW CHARTING METHOD TO DESCRIBE DIGITAL SYSTEMS
UNIV OF MISSOURI, ROLLA, PHD THESIS, 1973, 107 P;
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UNIV OF ILLINOIS, COORD SCIENCE LAB, MASTER'S THESIS, JUNE 1973,
60 P; ALSO REPT R-614; NTIS AD 766 747/ 0
- 109 PAGE, E.W.
PROGRAMMABLE ARRAY REALIZATIONS OF SEQUENTIAL MACHINES
DUKE UNIV, PHD THESIS, 1973, 156 P; SUP: P.N. MARINOS
DISS ABSTR, VOL 34, NO 9; UNIV MICROFILMS 74-7557
- 110 PAI, D.
A LOGIC DESIGN LANGUAGE FOR COMPUTER AIDED DESIGN
M. PHIL. THESIS, UNIV OF SOUTHAMPTON, 1971
- 111 PALMQUIST, S.R.
DELAY FREE REALIZATION OF ASYNCHRONOUS SEQUENTIAL SWITCHING
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UNIV OF ILLINOIS, COORD SCIENCE LAB, MASTER'S THESIS, JULY 1973,
41 P; ALSO REPT R-616; NTIS AD 766 748/ 8
- 112 PARNAS, D.L.
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PHD THESIS, CARNEGIE MELLON UNIV, DEPT OF EE, FEB 1965
- 113 PITT, D.A.
DESIGN OF TOTALLY SELF-CHECKING ASYNCHRONOUS SEQUENTIAL MACHINES
UNIV OF ILLINOIS, DEPT OF COMPUTER SCIENCE, MASTER'S THESIS, SEPT
1973, 39 P; ALSO REPT DCS-R-73-593; NTIS PB 224 540/ 50A
- 114 PLINER, M.S.
PDMS - A PRIMITIVE DATA BASE MANAGEMENT SYSTEM FOR REPRESENTING
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PHD THESIS, CASE WESTERN RESERVE UNIV, SEPT 1971, 264 PP;
DISS ABSTR, VOL 32, NO 8, P 4535B; UNIV MICROFILMS, NO 72-6325
- 115 PLISCH, D.C.
NEW RESULTS CONCERNING SEPARATION THEORY OF GRAPHS
PHD THESIS, UNIV OF WISCONSIN, 1970, 220 P
DISS ABSTR, VOL 31, NO 11, P 6616B; UNIV MICROFILMS 71-2234
- 116 POAGE, J.F.
THE DERIVATION OF OPTIMUM TESTS FOR LOGIC CIRCUITS
PHD THESIS, PRINCETON UNIV, 1963
- 117 POTASH, H.
A DIGITAL CONTROL DESIGN SYSTEM
PHD THESIS, UCLA, 1969, 248 PP, SUP G. ESTRIN; DISS ABSTR,
VOL 30, NO 8, P 3600B; UNIV MICROFILMS, NO 70-2246
ALSO: UCLA, REPT 69-21, MAY 1969
- 118 PUMPLIN, B.A.
A PROGRAMMING SYSTEM FOR THE SIMULATION OF DIGITAL MACHINES
PHD THESIS, IOWA STATE UNIV, 1971, 157 PP; SUP A.V. POHM;
DISS ABSTR, VOL 32, NO 8, P 4600B; UNIV MICROFILMS, NO 72-5249

- 119 RODE, M.A.
OPTIMIZING BOOLEAN EQUATION SIMPLIFICATION
PHD THESIS, UNIV OF CINCINNATI, 1969, 113 PP ; DISS ABSTR, VOL 30,
NO 11, P 5009B ; UNIV MICROFILMS, NO 70-9808
- 120 ROSE, C.W.
A SYSTEM OF REPRESENTATION FOR GENERAL PURPOSE DIGITAL COMPUTER
SYSTEMS
PHD THESIS, CASE WESTERN RESERVE UNIV, 1970, 208 PP ; DISS ABSTR,
VOL 32, NO 2, P 880B ; UNIV MICROFILMS, NO 70-19047
ALSO: REPT 1113, JENNINGS COMPUTER CENTER, CASE WESTERN RESERVE
UNIV, AUG 1970
- 121 ROSE, N.A.
COMPUTER-AIDED DESIGN OF PRINTED WIRING BOARDS
PHD THESIS, UNIV OF EDINBURGH, APRIL 1970
- 122 ROUSE, D.M.
A SIMULATION AND DIAGNOSIS SYSTEM INCORPORATING VARIOUS TIME DELAY
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PHD THESIS, UNIV OF MISSOURI, ROLLA, 1970, 145 PP ; DISS ABSTR,
VOL 31, NO 11, P 6618B ; UNIV MICROFILMS, NO 71-12320
- 123 ROY, B.K.
FAULT DETECTION AND DIAGNOSIS IN COMBINATIONAL CIRCUITS
OHIO UNIV, DEPT OF EL ENG, REPT EER-16-17, 177 PP , NOV 1972
(NTIS AD 754 029)
- 124 RUBIN, F.
PRINTED WIRE ROUTING FOR MULTILAYER CIRCUIT BOARDS
PHD THESIS, SYRACUSE UNIV, 1972, 308 PP
DISS ABSTR, VOL 33, NO 9, P 4236B; UNIV MICROFILMS 73-7767
- 125 RUSSELL, J.D.
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UNIV OF WISCONSIN, PHD THESIS, 1973, 177P; SUP: C.R. KIME;
DISS ABSTR, VOL 34, NO 9; UNIV MICROFILMS 73-27125
- 126 RUTMAN, R.A.
LOGIK: A SYNTAX-DIRECTED COMPILER FOR COMPUTER BIT-TIME SIMULATION
M.S. THESIS, UCLA, AUG 1964
- 127 RYNICKER, R.W.
MACHINE TRANSLATION OF A DIGITAL DESIGN LANGUAGE
M.S. THESIS, DEPT OF EL ENG, UNIV OF WISCONSIN, 1967
- 128 SALISBURY, A.B.
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STANFORD UNIV, PHD THESIS, 1973, 196 P;
DISS ABSTR, VOL 34, NO 9; UNIV MICROFILMS 74-6541
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MS THESIS, UNIV OF IDAHO, 1971
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ON THE REPRESENTATION OF DIGITAL FAULTS
PHD THESIS, UNIV OF ILLINOIS, 1969, 69 PP ; DISS ABSTR, VOL 30,
NO 7, P 3187B ; UNIV MICROFILMS, NO 70-968 ; ALSO: UNIV OF ILLINOIS,
CSL, REPT R-418 ; (NTIS AD 688 836)
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PHD THESIS, POLYTECHNIC INST OF BROOKLYN, 1971, 251 PP ;
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PHD THESIS, UNIV OF ILLINOIS, URBANA-CHAMPAIGN , 1970, 68 PP ;
DISS ABSTR, VOL 31, NO 9, P 5373B ; UNIV MICROFILMS NO 71-5231
- 135 SHAPIRO, G.N.
A FUNCTIONAL APPROACH TO STRUCTURED COMBINATIONAL LOGIC DESIGN
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UNIV OF ILLINOIS, DEPT OF COMPUTER SCIENCE, APRIL 1972, 121 P
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IMPLEMENTATION AND ANALYSIS OF EFFICIENT GRAPH PLANARITY TESTING
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DISS ABST, VOL 32, NO 8, P 4602B ; UNIV MICROFILMS, NO 72-7058
ALSO: REPT R-513, UNIV OF ILLINOIS, DEPT OF COMPUTER SCIENCE.
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- 139 SKITEK, D.G.
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ARIZONA STATE UNIV, PHD THESIS, 1973, 236 P; SUP: E.R.ROBBINS
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MIT, MASTER'S THESIS, 1966
- 141 SMITH, R.J.
SYNTHESIS HEURISTICS FOR LARGE ASYNCHRONOUS SEQUENTIAL CIRCUITS
PHD THESIS, UNIV OF MISSOURI, ROLLA, 1970, 88 PP ; DISS ABSTR,
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- 143 STORY, J.R.
STATE ASSIGNMENT OPTIMIZATION FOR SYNCHRONOUS SEQUENTIAL MACHINES
PHD THESIS, UNIV OF ALABAMA, 1971, 133 PP ; DISS ABSTR, VOL 32,
NO 1, P 949B ; UNIV MICROFILMS NO 71-20122
- 144 SU, Y.H.
COMPUTER ORIENTED ALGORITHMS FOR SYNTHETIZING MULTIPLE OUTPUT
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- 145 SUNG, C.H.
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PHD THESIS, UNIV OF TEXAS, AUSTIN, 1971, 80 PP ; SUP C.L.COATES;
DISS ABSTR, VOL 32, NO 11, P 6408B ; UNIV MICROFILMS NO 72-15842
- 146 SVISCO, N.J.
COMPUTERIZED LOGIC-ORIENTED DESIGN SYSTEM
AIR FORCE INST OF TECHNOLOGY, WRIGHT PATTERSON AFB, OHIO, SCHOOL
OF ENGINEERING, MASTER'S THESIS, JUNE 1973, 164 P;
ALSO REPT GE/EE/73S-6; NTIS AD 768 349/ 3GA

- 147 TAMMARU, E.
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PHD THESIS, STANFORD UNIV, 1968, 128 PP; UNIV MICROFILMS NO 69-301
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M.S. THESIS, UNIV OF ILLINOIS, 1970, ILLIAC IV DOCUMENT 211
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PHD THESIS, NORTHWESTERN UNIV, 1971, 76 PP; DISS ABSTR, VOL 32,
NO 9, P 5191B; UNIV MICROFILMS, NO 72-7847
- 150 TARJAN, R.E.
AN EFFICIENT PLANARITY ALGORITHM
PHD THESIS, STANFORD UNIV, NOV 1971, 160 PP, REPORT CS-244-71;
DISS ABSTR, VOL 32, NO 12, P 6974B; UNIV MICROFILMS, NO 72-16807
- 151 TAXIN, H.M.
INTERACTIVE GRAPHICS AND THE COMPUTER AIDED DESIGN OF DIGITAL
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PHD THESIS, UCLA 1970; ABSTRACT IN DISSERTATION ABSTRACTS
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- 152 TYLASKA, T.T.
FAULT DETECTION IN SEQUENTIAL MACHINES
PHD THESIS, UNIV OF HOUSTON, 1972, 177 PP; DISS ABSTR, VOL 33,
NO 9, P 4282B; UNIV MICROFILMS, NO 73-6365; ALSO,
REPT NUSC-TR-4421, NAVAL UNDERWATER SYSTEMS CENTER, NEWPORT, RI
(NTIS AD 750 266)
- 153 ULRICH, J.W.
A COMPUTATIONAL THEORY OF PLANAR IMBEDDING
PHD THESIS, UNIV OF TEXAS, AUSTIN, 1968
DISS ABSTR, VOL 19, P 3840B; UNIV MICROFILMS 69-6231
- 154 VANCELEMPUT, W.M.
AN INTERACTIVE SYSTEM FOR COMPUTER AIDED DESIGN OF PRINTED CIRCUIT
BOARDS
M.MATH THESIS, UNIV OF WATERLOO, DEPT OF APPLIED ANALYSIS AND
COMPUTER SCIENCE, DEC 1971; ALSO REPORT CSRR-2064
- 155 VLACK, D.
COMPUTER SIMULATION OF DIGITAL SYSTEMS ON THE HARDWARE LEVEL
PHD THESIS, CASE INST OF TECHNOLOGY, 1967, 193 P, SUP:H.W.MERGLER;
DISS ABSTR, VOL 28, NO 6, P 2435B; UNIV MICROFILMS 67-16108
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PHD THESIS, UNIV OF PENNSYLVANIA, 1971, 221PP; SUP H. YAMADA;
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PHD THESIS, SOUTHERN METHODIST UNIV, 1972, 136 PP (SUPERVISOR
S.A. SZYGENDA) ; DISSERTATION ABSTRACTS, VOL 33, NO 9, P 4236B,
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1. Modelling philosophy for digital system.
2. Computer-aided analysis (determinacy, deadlocks).
3. Languages for computer-aided logic/system design.
4. Hardware compiler (translation of design languages).
5. System level simulation.
6. Logic syntheses.
7. Logic level simulation
8. Partitioning, card selection, placement and routing.
9. A complete, interactive design automation system.
10. Recent development in computer-aided analysis and design of digital systems.
11. Future trend in design automation.

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Detection and location of single and location of single multiple failures in digital networks. Efficient algorithms for generating tests for testing permanent and transient faults. Design of diagnosable networks, design to simplify testing. Introduction to the design of fault-tolerant systems including static, dynamic redundancy. Fail-soft digital systems. Testing redundant networks. Recent development and future trends in fault diagnosis.

COURSE OUTLINE:

1. Overview and recent development in fault diagnosis.
2. Fault diagnosis of combinational networks.
3. Fault diagnosis of sequential networks.
4. Detection and location of multiple faults.
5. Transient failures and non-struck type faults.
6. Design of fault-tolerant and fail-soft digital systems.
7. Identification of redundant components in digital systems
8. Identification of indistinguishable faults.
9. Design of diagnosable digital networks.
10. Fault location of digital systems with redundancy.
11. Self-repair computers.
12. Future trend on fault-tolerant computing and fault diagnosis.

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